HIGH PERFOMANCE ALU DESIGN - A PAPER REVIEW

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ABSTRACT: ***Arithmetic Logic Unit is of core significance in digital technologies as it is an integral part of central processing unit. ALU is capable of calculating the results of a wide variety of basic arithmetical and logical computations. Binary addition is one of the greatest primitive and commonly used applications in computer arithmetic operation. Parallel Prefix Adders have been established as the most efficient circuits for binary addition. The energy efficient designs have gained more recent attention and for highly employed functional units, especially for the adders. The energy consumption of an adder depends on the circuit minimizing, the addition procedure, the recurrence structure and the wiring complexity. The proposed work gives the performance evaluation of addition algorithms on Kogge-Stone arrangement and has been observed to save energy by the proper selection of addition algorithms in 8-bit adders. Kogge-Stone (KS) adder is one of the high performances and minimum depth parallel prefix adder arrangement design. The VHDL implementation of 8-bit arithmetic logic unit (ALU) is proposed using high speed adder. The design was implemented using VHDL Xilinx Synthesis tool ISE and targeted for Spartan device.***

Key words: Parallel prefix adder, Kogge-stone adder, VHDL, Xilinx synthesis tool ISE, Spartan devices

I. INTRODUCTION

Segmentation is the initial process used for the partitioning of images into different parts. It will help to change the representation of an image which will be easy to analyze. It occurs as a set of regions that collectively represents the complete image. The images are scanned by Magnetic Resonance Imaging (MRI) scan (or) Computer Tomography (CT) scan. The MRI scan is preferred more than that of the CT scan because of its easy diagnosis.

The image segmentation algorithms such as K-means algorithm, K-means integrated with Fuzzy C-means (KIFCM) algorithm, Otsu's algorithm, EM, MEM (Modified Expectation of Maximum), SOM (Self Organising Map), etc., were widely used and they are compared based on their performance. These features with some important parameters are studied and compared to give a clear idea about the different techniques used for image segmentation.

II. ALU DESGIN – CLASSIFICATIONS

The image segmentation is mainly classified into the following three types

Operation Type:

a) Structural segmentation:

The structural segmentation method mainly focusses on the particular region or only the required region that have to be segmented.

b) Stochastic Segmentation:

The stochastic segmentation method will focus on the discrete pixel values and not the structural information of the image or region.

c) Hybrid Segmentation:

The hybrid segmentation method will include both the structural segmentation as well as stochastic segmentation.

III. ALU DESGIN – METHODS

The most popular techniques used for image segmentation are: thresholding techniques, edge detection-based techniques, region-based techniques, clustering based techniques, watershed-based techniques, partial differential equation based and artificial neural network-based techniques etc. These all techniques are different from each other with respect to the method used by

these for segmentation.

1) *VEDIC MATHEMATICS*:

Vedic multiplier-based design of multiply and accumulate unit by employing Urdhva Tiryagbhyam Sutra. Further, it implements an efficacious ALU with 32-bit architecture. Simulation analysis disclosed the comparison of proposed 32-bit ALU with existing architectures. In addition, complexity in hardware, area and delay reduction multiplier

2) 8 BIT ALU CHIP & MUX:

8 bit ALU chip has been design to the benefits of all the computations are done in parallel and available simultaneously, so no clock resources are wasted. The MUX is then used to select the required output. As a fundamental part of the microprocessors, ALU performs computing operations and it is typically on the critical path. Therefore, the achievable operating frequency of the whole microprocessor is determined by the operating speed of ALU. At the same time, ALU is also one of the most active components in microprocessor, raising the power and thermal issues. Therefore, the lowest voltage supply to the circuit is needed to reduce power and reducing the propagation delay is required to enhance the speed of the ALU.

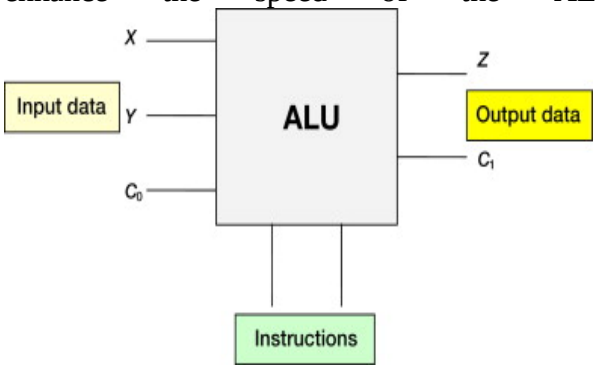

Figure 2 *ALU Output*

3) HALF ADDER USING AVL TECHNOLOGY:

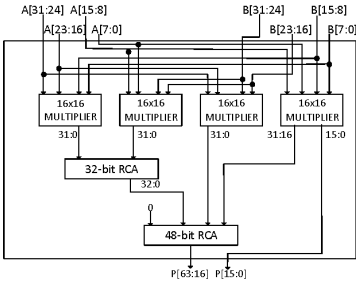

Figure 1: *Architecture diagram of 32x32 bit Vedic Wallace based multiplier*

A traditional half adder circuit design for power optimization is a technique used in low voltage applications half adder circuit design using Adaptive Voltage Level (AVL) techniques. When compared to conventional design circuits, AVL techniques consumed less power. AVL techniques, the ground potential raises with the help of adaptive voltage level at ground (AVLG) techniques, the supply potential raises with the help of adaptive voltage level at supply (AVLS). Using both techniques the half adder circuit design required 9T transistors When compared to CMOS and conventional Half Adders, this design consumes less power, has a shorter propagation delay, and takes up less space on the layout. Layout cell, Simulation result, MOS characteristic, and Power vs Supply Voltage Variation

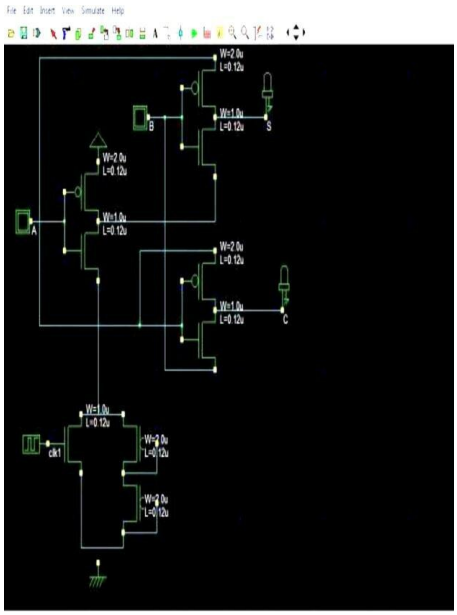

Figure 3 Half Adder Circuit diagram using the AVLG Techniques

4) 16-BIT ARCA SQRT CSLA DESIGN*:*

6-bit ARCA SQRT CSLA architecture and its layout using addone ripple carry adder (ARCA) and carry enable (CE) modules for optimizing the delay, area and power consumption than the existing 16-bit regular SQRT CSLA. The proposed architecture has fIve groups for area and delay estimation. The proposed m-bit ARCA module is used in this research instead of using mbit RCA when Cin = 1, where m = 2, 3, 4, 5. The proposed m-bit ARCA module has (m − 1) number of FAs and one addone (A-1) logic module. This section focuses on evaluating the proposed modification in group 5 of the 16-bit CEBEC SQRT CSLA architecture shown in for the estimation of delay and area. The delay and area evaluation methodology considers all gatesmade up of AND, OR and inverter (basic logic gates), each having a delay of one unit and an area of one unit. The number of gates for delay in the longest path of each logic block contributes to the maximum delay and the area evaluation by counting the total number of basic gates required for each logic block.

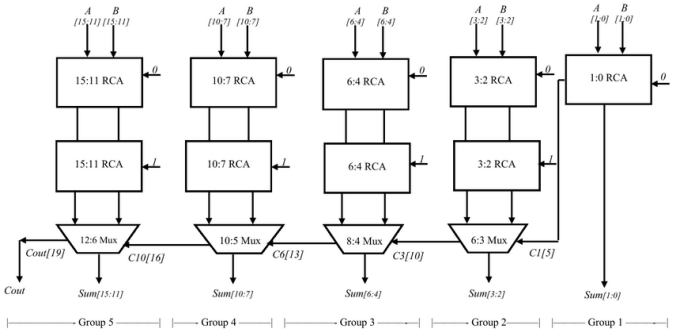

Figure 4 Architecture of the proposed 16-bit ARCA SQRT CSLA

5) High-Performance ALU Design Using Prospective Single Electron Transistor:

The arithmetic logic unit (ALU) is one of the most essential components of any microprocessor or computing system that is capable of performing several arithmetic as well as logic operations. For realizing efficient and high-performance ALU, proper designing, optimum selection of materials and incorporation of advanced devices are utmost important. The single electron structure for achieving high-end computing system. In this paper, the prospective SET-based ALU is realized to meet next-generation requirements like higher speed, lower power, and volume. Also, the enhancement capability of ALU can be further

accomplished by incorporating effective modular design using slice-based approach. The slice-based design approach provides simplicity and extensibility of the design. In this, each slice has the capability to perform arithmetic and logical

operations on one-bit input data. Henceforth, cascading of n such slices generates the n-bit ALU. The multiplication operation is executed separately. The incorporation of separate multiplier block aids in achieving fast execution of multiplication operation with a single instruction. The performance of high-end proposed SET-based ALU

ALU Designs	Principle	Advantages	Disadvantages
Vedic mathematics	implementation of multiply	faster, small, number reproduction, number increments	complicated due to heavy copies
8 bit ALU chip & mux:	carry select line	Reduce cost and complexity, simple logic.	limitations on the number of ports, delays are required for switching gates
Half adder using avl technology	In integrated circuit design, a half-adder that performs an arithmetic operation on two binary numbers.	Compared to CMOS and traditional semiconductors, this design consumes less power, has a shorter propagation delay and takes up less layout spac	A minimum voltage supply to the circuit is required to reduce power and a reduction in propagation delay is required to increase the speed of the ALU.
16-bit arca sqrt csla design	It was developed using Verilog HDL. Using Xilinx 14.1, it is simulated and synthesized	redundant logic, partial sharing of logic, more energy and area efficient,	small carrying performance delay, power loss than CSLA
High-Performance ALU Design Using Prospective Single Electron Transistor*:*	Utilizing the behaviour of single electron tunneling in nanoscale transistor	The inclusion of separate multiplication blocks helps to achieve a fast multiplication operation with a single instruction.	Fabrication challengers, sensitivity to noise and temperature, limited scalability

is compared with the conventional complementary metal oxide semiconductor (CMOS) and 18 nm FinFET technology-based ALU designs. It is observed that the SET-based ALU gives 1.9× lesser delay and 19.8× lower power dissipation as compared to its 16 nm CMOS counterpart. Also, with respect to 18 nm FinFET-based technology, proposed SET-based design out-stands extensively in terms of lower transistor count and power.

II. ALU DESIGNS - A COMPARISON

II. CONCLUSION

In this review of different Adder techniques, various ALU design techniques were described and compared. These techniques were suitable for many applications.

REFERENCES

[1] Sravani, Y., & Rameswarudu, E. S. IMPLEMENTATION OF ERROR DETECTABLE CSA FOR ARTIFICIAL INTELLIGENCE APPLICATIONS WITH EASY TESTABILITY.

[2] Sasamal, TrailokyaNath, Ashutosh Kumar Singh, and Anand Mohan. "Design of Arithmetic Logic Unit in QCA." In Quantum-Dot Cellular Automata Based Digital Logic Circuits: A Design Perspective, pp. 107-117. Springer, Singapore, 2020.

[3] Korkmaz, M. (2021). Energy-Efficient Transaction Scheduling in Data Systems.

[4] Costa, N., Sánchez, L., & Couso, I. (2021). Semi-Supervised Recurrent Variational Autoencoder Approach for Visual Diagnosis of Atrial Fibrillation. IEEE Access, 9, 40227-40239.

[5] Liu, R., Ramli, A. A., Zhang, H., Datta, E., & Liu, X. (2021). An Overview of Human Activity Recognition Using Wearable Sensors: Healthcare and Artificial Intelligence. arXiv preprint arXiv:2103.15990.

[6] Rathi, Mrs Leena. "Ancient Vedic Multiplication Based Optimized High Speed Arithmetic Logic." International Journal of New Practices in Management and Engineering 3, no. 03 (2014): 01-06.

[7] Kaur, Navdeep, Neeru Malhotra, and Balwinder Singh. "VHDL Implementation of ALU with Built In Self Test."

[8] Nori, Suha M., and Shefa A. Dawwd. "Reduced Area and Low Power Implementation of FFT/IFFT Processor." Iraqi Journal for Electrical And Electronic Engineering 14, no. 2 (2018): 108-119.

[9] Deshmukh, V. V., & Chorage, S. S. (2021). Non-invasive determination of blood glucose level using narrowband microwave sensor. Journal of Ambient Intelligence and Humanized Computing, 1-16.

[10] Miah, M. S., Hossain, M. A., Ahmed, K. M., Rahman, M. M., & Calhan, A. (2021). An Energy Efficient Cooperative Spectrum Sensing for Cognitive Radio-Internet of Things with Interference Constraints.

[11] Kumar, V. K., & Rai, C. S. (2021). Efficient Implementation of Cryptographic Arithmetic Primitives Using Reversible Logic and Vedic Mathematics. Journal of The Institution of Engineers (India): Series B, 102(1), 59-74.

[12] Gowthami, M., Jalall, K., & Kiruthika, K. (2021, March). High Speed and Performance analysis of Multiplier in Field Programming Gate Array. In IOP Conference Series: Materials Science and Engineering (Vol. 1084, No. 1, p. 012062). IOP Publishing.

[13] Rohith, S., Babu, K. R., & Chandrashekar, M. N. FPGA Implementation of 8-Bit Vedic Multiplier for DIT-FFT Application Using Urdhva Tiryagbhyam Sutra.

[14] Harish, B., Rukmini, M. S. S., & Sivani, K. (2021). Design of MAC unit for digital filters in signal processing and communication. International Journal of Speech Technology, 1-5.

[15] Gowreesrinivas, K. V., & Punniakodi, S. (2021). Improvised hierarchy of Floating Point Multiplication using 5: 3 Compressor. International Journal of Electronics Letters.

SIA Roadmap, http://www.sematech.org/public/roadmap/doc

[16] Sakurai, T.: Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSI's. IEEE Trans. Electron Devices 40, 118–124 (1993)

[17] Adler, V., Friedman, E.G.: Delay and power expressions for a CMOS inverter driving a resistive-capacitive load. Analog Integrat. Circuits Signal Process 14, 29–39 (1997)

[18] Al-Assadi, W., Jayasumana, A.P., Malaiya, Y.K.: Pass-transistor logic design. International Electron Journal 70, 739–749 (1991)

[19] Morgenshtein, A., Fish, A., Wagner, I.A.: Gate-Diffusion Input (GDI) – A Power Efficient Method for Digital Combinatorial Circuits. IEEE Trans. on VLSI 10, 566–581 (2002)

[20] Alidina, M., Monteiro, J., Devadas, S., Ghosh, A., Papaefthymiou, M.: PrecomputationBased Sequential Logic Optimization for Low Power. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2(4), 426–435 (1994)

[21] Tenenbaum, A.: Structured Computer Organization, 4th edn. Prentice-Hall of India (1999)

[22] Chandrakasan, A.P., Sheng, S., Brodersen, R.W.: Low- power CMOS digital design. IEEE

J. Solid-State Circuits 27, 473–484 (1992)
[23] Chandrakasan, A.P., Brodersen, R.W.: Minimizing power consumption in digital CMOS
circuits. Proc. IEEE 83, 498–523 (1995)
[24] Morgenshtein, A., Fish, A., Wagner, I.A.: Gate-Diffusion Input (GDI) – A Technique for
Low Power Design of Digital Circuits: Analysis and Characterization. In: ISCAS 2002,
USA (May 2002)