Design and Analysis of Vertical Tunneling Dual Material Double Gate Tunnel Field Effect Transistor (VTDMDG-TFET)

B. Balaji[1], G. Vedavyas[2], D. Tanish[3], M. Lohith[4], J. Gopi[5], Shaik Hameed Basha[6]

Department of Electronics and Communication Engineering, Koneru lakshmaiah Education Foundation, Green Fields, Vaddeswaram, Guntur (Dt), Andhrapradesh-522502, India

vahividi@gmail.com, vedavyasg2000@gmail.com, shaikhameed1234@gmail.com, tanishlogo@gmail.com , lohithkumar1507@gmail.com , jangalagopi1122000@gmail.com

ABSTRACT:

In this paper, we observed the characteristics of vertical tunneling field effect transistors and performed biosensor application using the analysis of germanium-silicon VTFET. The operation of the vertical tunneling field effect transistor is different when compared to the lateral tunneling field effect transistor in the tunneling field effect transistors the tunneling process happens based on the B to B tunneling. But the direction of the tunneling happens in the tunneling field effect transistors are not the same. The vertical tunneling field effect transistors have more lead compared to the L-tunneling FET. The dual material double gate tunneling technique (VTDMDG-TFET) is developed to improve the properties like capability of current driving, swing of subthreshold, and ratio of switching, in the vertical tunneling field effect transistor. The different dielectric materials are being suggested in vertical tunnel field effect transistors (VTFET). In these Germanium (Ge) acts as source material and Silicon (Si) acts as drain material to enhance the ON-state current. The enhancement of heterojunction to the carrier tunneling can be done at the source channel junction. There are several states are obtained for the increment of the carrier tunneling. The heightening of suggested Ge-Si obtained Vertical tunneling field effect transistors (considering analog /Radiofrequency measures) against the regular Vertical tunneling field effect transistors. The biosensor application is operated by the N+ pocket doping method, With the help of an electric field, electrostatic potential and drain current with verified simulated device data. In performing biosensor application, it is important to consider a germane material and structure like a HDB-VTFET. It made a drastic change on every parameter of the device like in low off-current state crackdown on the ambipolar behavior. This model consists of both dielectric constant, charge and proper solution application for neutral and charged biomolecules.

1. INTRODUCTION

The main cause for moving from MOSFETS to vertical field effect transistors is while performing scaling in metal oxide field effect transistors [1] it reaches Nano-meter dimensions, while doing further scaling in Nano-meter dimensions [2] the short channel effects are becoming a major problem[3], and gives many problems like gate leakage currents, source to channel electrostatic coupling, etc.[4]. To control all these problems the new device was designed with new configurations which will be having different operations compared to the metal oxide FET which is a tunneling field effect transistor. Unlike the regular transistor, the tunnel field effect transistor with inverse materials of source and drain regions. The operations of tunnel field effect transistors depend upon interned tunneling [5].

As we are taking into consideration of solid barrier problem. The forbidden band is situated in between the conduction and valence bands, where the mobility of carriers would have happened among the two bands. So, carrier tunneling is performed in between the conduction band and valence band. But compared with the drain region, the interfering concentration of the source region is more which can enhance the drive current [6]. then the charge and discharge of the capacitance can be done very quickly.

The germanium material has high mobility, Interbrand tunneling, and low band gap. so, it is used as a source region to improve ON-state current. As we are decreasing the tunneling barrier at the source side also increases the current of ON-state. The ambipolar

behavior which can be able to sense the biomolecules when the negative field is applied at the short channel effect gains immunity to the Tunnel field effective transistor. Nowadays biomedical diagnosis equipment based on FETs has become handier for the implementation of sensitive, label-free, and fast response products [7]. With the help of CMOS fabrication, miniaturization, higher sensitivity, and feasibility FETs are showing much more impact on the healthcare industry. FET-based biosensors faced several effects such as a shorter length effect and larger sub-threshold swings [8]. To overcome those disadvantages, biosensors based on TFET with more sensitivity and with accurate working progress have been introduced by so many researchers because of the band-to-band tunneling(B-B) approach. However, TFETs also has some merits like low "ON" current, am bipolarity effect, and low I_{ON}/I_{OFF}. To overcome these disadvantages some architectures have been introduced by researchers such as the dielectric-modulated heterostructure Tunnel field effect transistor biosensors, DM dual gate Tunnel FET biosensors, and Dielectric modulated shortage biosensors [9]. We can use VTFET-based biosensors more perfectly compared to MOSFET-based biosensors.

2. DEVICE CONCEPT:

The main difference between the lateral tunneling FET and vertical TFET is the direction of the tunneling happens about the oxide surface. In the lateral tunneling field effect transistor, the tunneling happens lateral (parallel) to the oxide surface [10], whereas in the other tunneling FET the tunneling happens vertically to the oxide surface.

2.1. Schematic Diagram (LTFET):

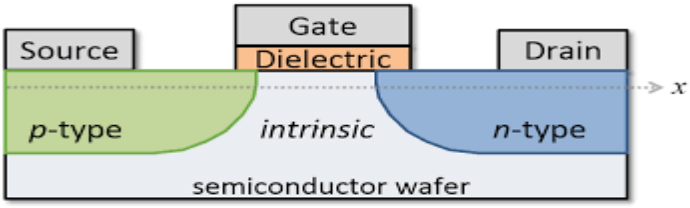


Figure [1.1] The schematic of TFET

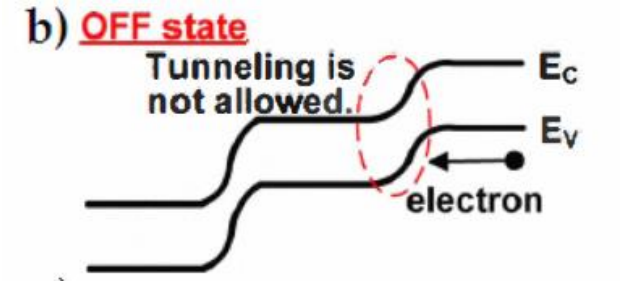


Figure [1.2] OFF-state band diagram

In the above figure[1.2] we have shown the band diagram of lateral field effect transistor, when voltage supplied to gate is less than the minimum threshold voltage, the transistor will lie in OFF-state.Tunneling boundary is becoming large, so tunneling cannot happen in an off state and we can observe only leakage current[11].

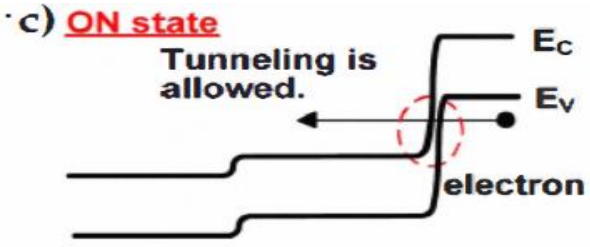


Figure [1.3] Band diagram of the lateral TFET.

In the above figure[1.3] we have shown, band diagram when the gate voltage is greater than the threshold level, the transistor will be in the state. In the state, the tunneling boundary will become close and it allows the band-to-band tunneling to happen.

The problem in the lateral tunneling field effect transistor is the gate voltage cannot control the drain current, this problem in the lateral tunneling field effect transistors had already been verified experimentally [12].

After considering the drawbacks of the LTFET, a new device had constructed that is VTFET. In a vertical tunneling field effect transistor, process of tunneling happens parallel to the oxide surface. By changing the direction of the tunneling happens, gate voltage in the vertical tunneling field effect transistors can directly operate the tunneling [13]. By this new operation, we can get less sub-threshold swing and higher on-current when compared to the other type of field effect transistor.

2.2. VTDMDG-TFET-Vertical tunneling-based dual material double gate tunneling field effect transistor.

To improve the properties like current driving capability, switching ratio, and subthreshold swing in a normal vertical tunneling field effect transistor, a new vertical tunneling field effect transistor is developed that is vertical direction of tunneling based two material dual gate tunneling field effect transistor. This proposed device structure has an increment in terms of work function engineering, a gate oxide material, gate length, output characteristics, and Si-thickness when compared to the normal vertical tunneling field effect transistor [14]. A combination of two metal gates, namely an auxiliary gate and tunnel gate will be there in the gate terminal in Vertical tunneling based dual material double gate tunneling transistor, by using the dual material at the gate terminal constructs the new device structure (VTDMDG-TFET) capable in terms of high on-current, optimized subthreshold swing as well as high switching ratio. To improve the on-current of this new device, higher dielectric material oxide (Hfo_2) is used as the gate dielectric material oxide [15].

3 .DEVICE STRUCURE:

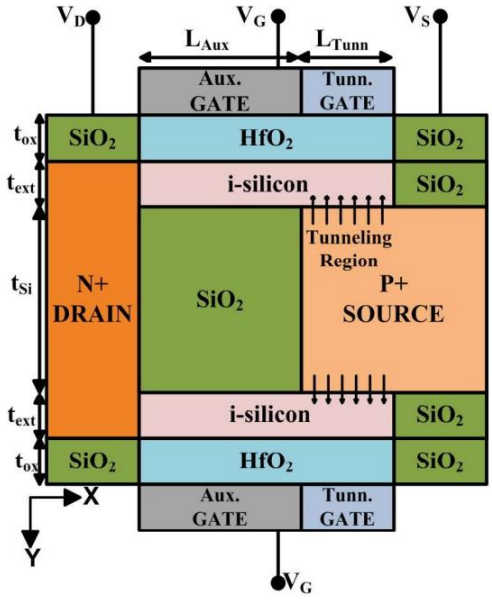


Figure [2] schematic representation of proposed VTDMDG-TFET

As we know VTDMDG-TFET shown in the figure [2] consists of dual metal gates namely, the first gate (AUX) and the second gate (TUNN) which are used to increase the on-current. The gate structure which is present at the source side is called the tunnel gate and another gate structure that is present at the drain side is called the auxiliary gate [16]. The tunnel gate controls the on-current (I_{on}) and the auxiliary gate controls the leakage current (I_{of}).

3.1. Analysis of gate work function:

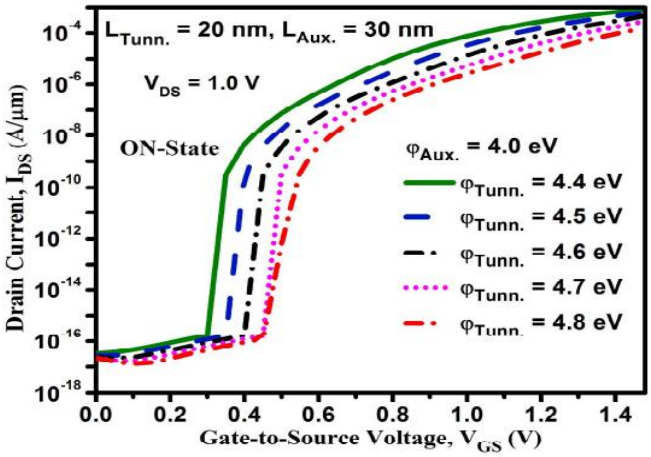


Figure [2.1] I_{DS} –V_{GS} plots for different tunnel gate work-function at constant b_{4i} = 4eV $L_{Tunn.}$ =20 nm and $L_{Aux.}$ =30 nm in ON-state.

In the above plot figure [2.1], we considered the work function of auxiliary gate constant at 4.0ev and further increased the tunnel gate work function from 4.4ev to 4.8ev., then by doing these variations we can observe the changes in drain current (Vgs) for increasing gate to source voltage (Vgs) from the above plot[17]. we can observe that when Tonn=4.4ev, higher on-current had achieved. In the same way, the drain current is pulled out from the Ids-Vgs characteristics by considering the constant tunnel gate work function at Tonn=4.4ev and varying the work function of the auxiliary gate [18].The below plot represents the variations by considering the above work function values.

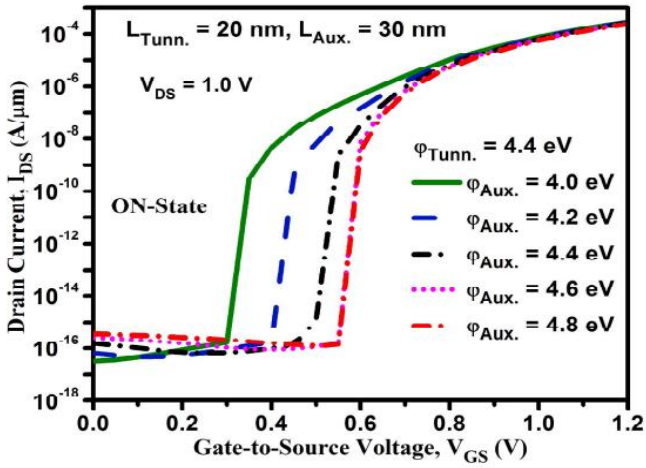


Figure [2.3] I_{DS} –V_{GS} plots for the variations in the auxiliary gate work-function at constant Φ_{Tunn} . =4.4 eV, in ON-state.

The DC parameters results for varying auxiliary gate functions. In this case, we found the lowest leakage current. By considering the above two plots we can state that the highest on-current and highest 0ff-current are achieved at Aux=4.0ev and Tun=4.4ev. So far, we

have proved that high on current and off current, coming to the subthreshold swing [19]. So, the suitable gate work function values for device design are Aux=4.0ev and Tunn=4.4ev.

As per the requirement of high steep Subthreshold swing devices and high on-current, the proposed device structure Vertical tunneling based double material with two gate tunneling field effect transistor has been proposed with the simulation results. VTDMDG-TFET is the best device for ultralow-power applications in the analog domain.

3.2. Energy Band Profile in Germanium –Silicon Vertical tunneling field effective transistor:

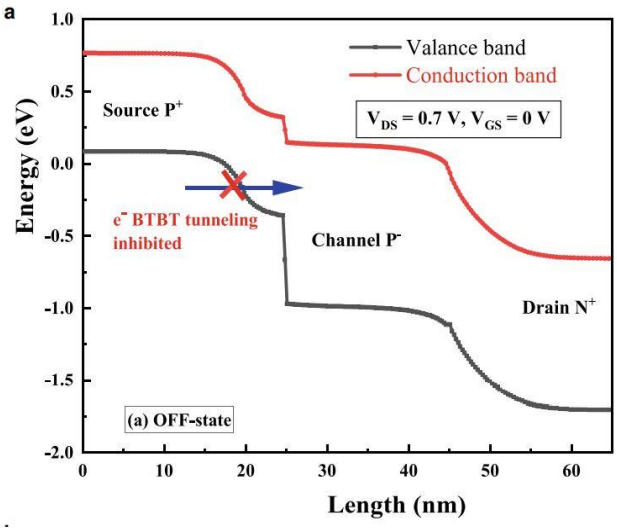
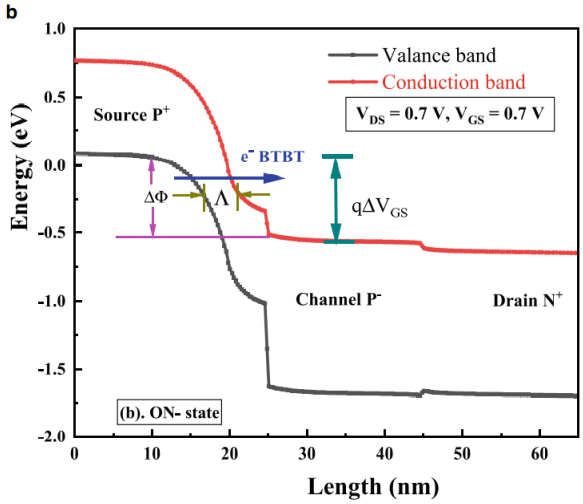


Figure [3.1] Band profile in OFF state



Figure[3.2] Band profile along the device length ON state

In short channel junction as the mobility of carrier takes place then it is denoted as the tunneling width(^) and the deviations occurred in the valence region at the p+ region and conduction region at the channel p- region, then that indicates tunneling window (ΔΦ)[20]. In this study, if the carriers are put a stop for their mobility in the short channel junction, then it shows a low current. At that time lower level of the current in the OFF-condition than in the ON- condition. As we are increasing the gate voltage level then the maximal ON-state current value is 5.55 x 10^-5 Ampere/micrometer and the maximal OFF-state current value is 2.12 x 10^-17 Ampere/micrometer[21]. Here figure 3.1 indicates the analytical graph of the energy band in OFF-state current and figure 3.2

indicates the analytical graph of the energy band of the ON-state current. The resulting ratio of the ON-state current and OFF-state current is 2.61 x 10^12(Ion/Ioff).

3.3. Proposed Ge-Si Vertical tunnel field effective transistors:

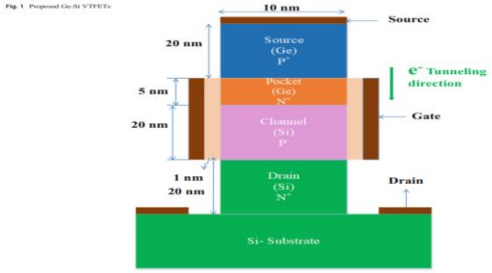


Figure [4] Proposed Ge-Si VTFETs

The drain (Si) region(N+) length of the Vertical tunnel field effective transistor is 20nm.

The source (Ge) region(P+) length of the Vertical tunnel field effective transistor is 20nm.

The channel (Si) length of the Vertical tunnel field effective transistor is 20nm.

The channel thickness of the Vertical tunnel field effective transistor is 10nm.

The source pocket (Ge) length is 5nm with an oxide thickness of 1nm[22] in the figure[4].

The buried oxide vertical tunnel field effective transistor is proposed for Hetero dielectric vertical tunnel field effective transistor (HDB-VTFET), Underlapped channel drains buried oxide vertical tunnel field effective transistor((UCD)HDB-VTFET) and Channel drain Hetero dielectric buried oxide vertical TFET((CD)HDB-VTFET).

Hetero dielectric buried oxide vertical tunnel field effective transistor (HDB-VTFET) is for improving the drive current in biosensor application more than the V-tunnel field effective transistor (VTFET)[23].

There was a huge change in working performance of the Hetero dielectric buried oxide vertical tunnel field effective transistor than vertical tunnel field effective transistor on parameters like lowering of drain induced barrier, On state current, crack down on the ambipolar behavior during the lesser off-state current and the Subthreshold slope.

3.4. The transfer characteristics of (HDB-VTFET), Underlapped channel drain vertical tunnel field effective transistor((UCD)HDB-VTFET) and Channel drain Hetero dielectric buried oxide VTFET((CD)HDB-VTFET) on different BOX lengths.

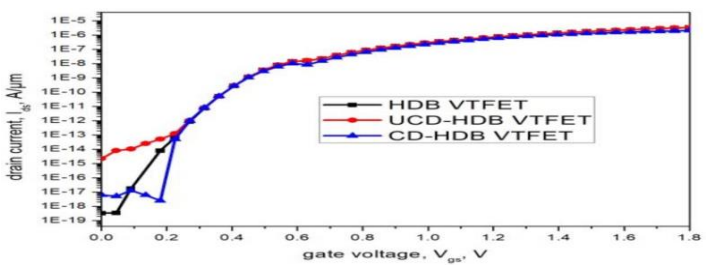


Figure [4.1] Calibration of I_D vs V_{GS} against Reference

In the above figure [4.1] comparing the 3 vertical tunnel field effective transistors, the Hetero dielectric buried oxide V-tunnel field effective transistor24] strives the drive current consistently on low gate voltage (Vgs).

3.5. The ambipolar behavior characteristics of the Hetero dielectric buried oxide vertical tunnel field effective transistor (HDB-VTFET), Underlapped channel drain Hetero dielectric buried oxide vertical tunnel field effective transistor((UCD)HDB-VTFET) and Channel drain Hetero dielectric buried oxide vertical tunnel field effective transistor on different BOX lengths.

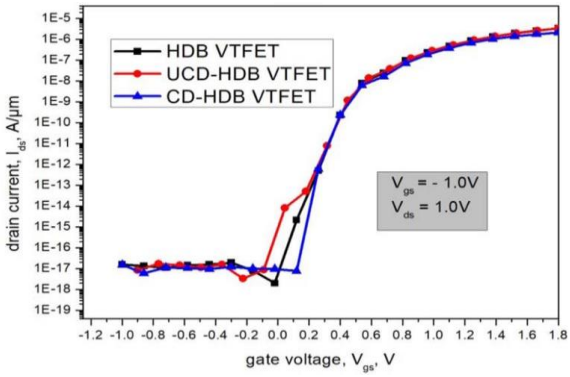
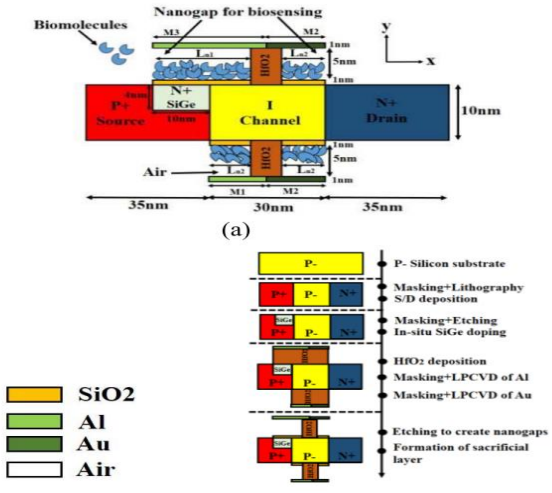


Figure [4.2] Characteristics of Ge-Si VTFETs

This ambipolar behavior characteristics graph on different BOX lengths shows the results in producing the unit of drain voltage and gate voltage [25].

As compared with the 3 devices the Hetero dielectric vertical tunnel FET gives beneficiary results than the Underlapped channel drain Hetero dielectric buried oxide vertical tunnel field effective transistor((UCD)HDB-VTFET) and Channel drain Hetero dielectric buried oxide vertical tunnel field effective transistor((CD)HDB-VTFET).

4. ARCHITECTURE, SIMULATION SETUP FOR BIOSENSING APPLICATION:



(b)

Figure [5] (a) is a 2-Dimensional schematic of VTFET biosensor which is embedded with nanogap, and figure (b) is a fabrication flow [26].

In the above figure [5] the architecture of nanogap embedded doped with N+ pocket Vertical TFET can be seen in the 2-D cross-sectional view VTFET is dopped with SiGe N+ doping, 30% Ge concentration with the concentration of 1 x 10^{19} Cm^{-3} - n-type all over the simulation. The gate oxide is perpendicular to the BTBT in the presence of Silicon-Germanium N+ pocket doping by adding it to lateral tunneling. With the length of constant dielectric material (HfO_2) is 10nm. The thickness of Silicon-Germanium is 1 nm is proposed to the reduce the leakage current and sensitivity degradation.

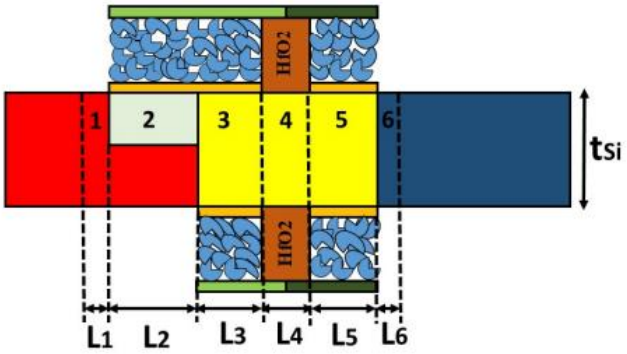


Figure [6] Schematic of the introduced biosensor showing various regions for model derivation. Comparison between the modeled and simulated surface potential profile at 0.2 nm below y = tS

In the above figure [6], the Nano gap for biosensing is filled with biomolecules. As we can see in the above figure, VTFET is divided into six regions they are (L_1, L2, L3, L4, L5, and L_6) including source/drain side depletion.

5. RESULTS

In Germanium-Silicon vertical tunneling field effective transistor the capacitance may get some disturbances in the circuit due to holding the higher frequency [27]. The GCD will decreases in the orderliness of the Silicon-Germanium vertical tunneling field effective transistor than the gate to the source capacitance. Both capacitances are dependent on the Gate voltage (Vgs).

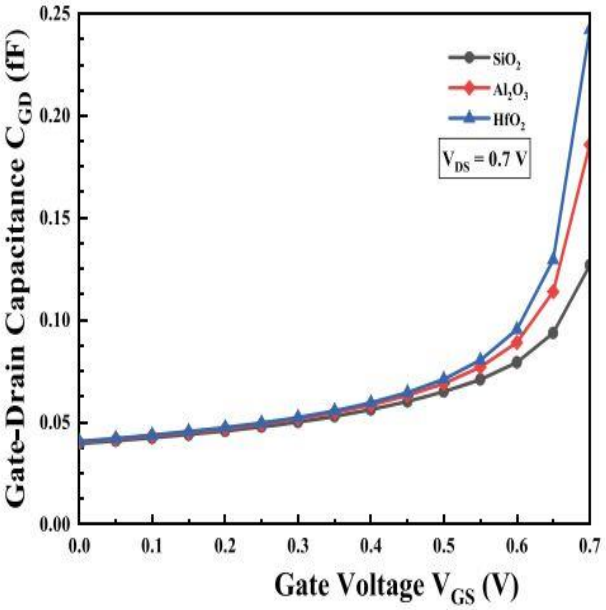
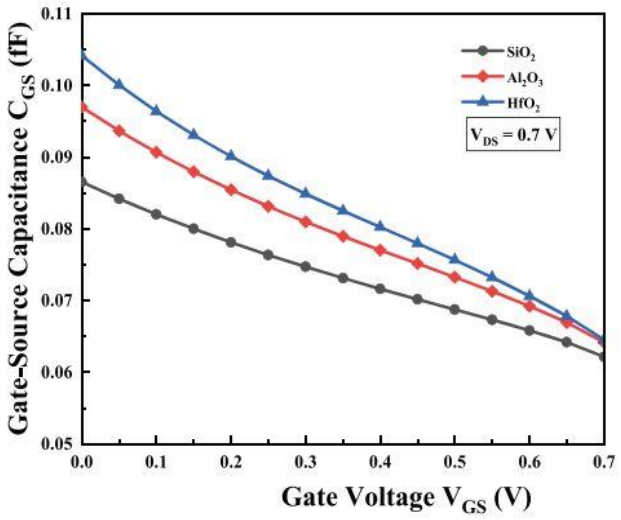


Figure [7] C_{GD} vs V_{GS} of Ge-Si



Figure[8] C_{GS} vs V_{GS} of Ge-Si VTFET

In the above figure[8], The prospective barrier of the source-channel and drain channel junction rises and decreases in order due to increasing the gate voltage (Vgs)[29] .On high-frequency response, the Gate to the drain capacitance (CGD) dominates the Gate to the source capacitance (CGS) in the vertical tunneling field effective transistor.

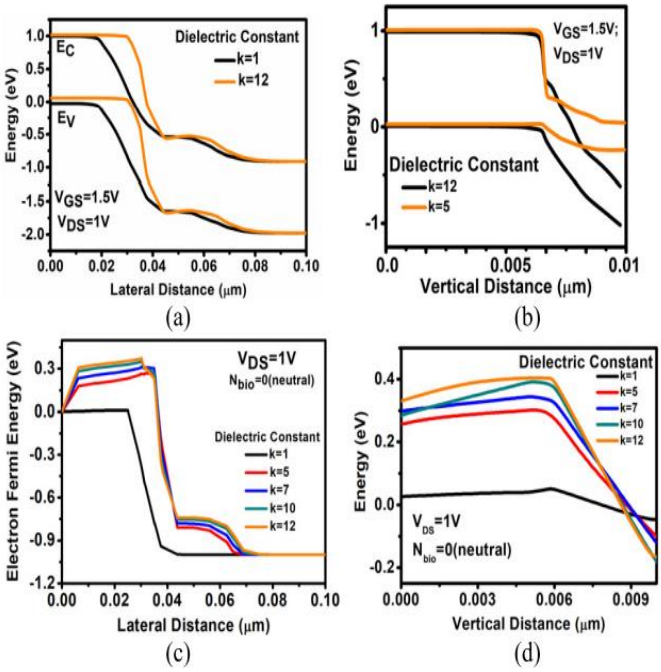


Figure [9] Band diagram at VGS = 1.5V for normal biomolecules having k = 1 and 12 for the lateral direction and the vertical direction, and corresponding electron Fermi energy at (c) lateral direction, and (d) vertical direction.

In the above Figure [9], we can see the energy band diagram variations due to different biomolecules in the lateral direction. When k = 12, we can see there is more bandgap in the drain current.

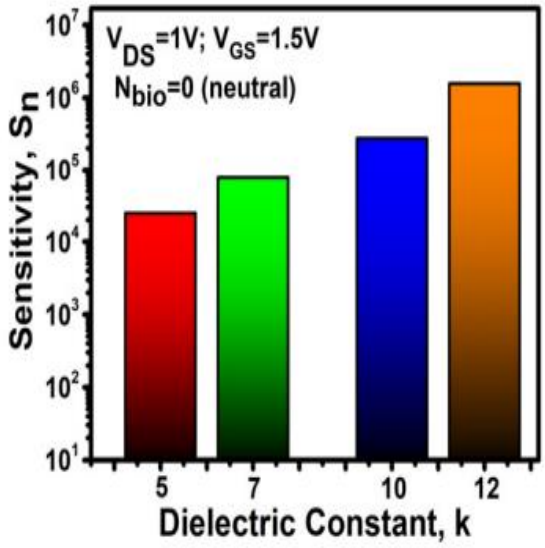


Figure [10] Sensitivity versus neutral biomolecules for dielectric constant k = 5, 7, 10, and 12.

In the above figure [10], we can see the sensitivity of versus biomolecules for dielectric constant.

CONCLUSION

Through this study, we can understand the advantages of the vertical tunneling field effect transistor over the lateral tunneling field effect transistor. Vertical based tunneling dual material dual gate tunneling field effect transistor is the best device for ultralow-power applications in the analog domain. In vertical tunneling field effect transistor, the valence band and conduction band energy analysis were represented for performing the analysis of higher frequencies in capacitances, the capacitance from gate to drain (CGD) becomes the dominant component than the Gate to source (CCGs)[30]. More than the regular vertical tunnel field effective transistor the (HDB-VTFET) gives exceptionally energy productive integrated circuits and learned about the working principle of VTFET-based biosensor.

References:

[1] D. Sarkar and K. Banerjee, "Proposal for tunnel-field-effect-transistor as ultra-sensitive and label-free biosensors," Appl. Phys. Lett., vol. 100, no. 14, Apr. 2012, Art. no. 143108.

[2] H. Im, X.-J. Huang, B. Gu, and Y.-K. Choi, "A dielectric-modulated field-effect transistor for biosensing," Nature Nanotechnol., vol. 2, no. 7, pp. 430–434, Jul. 2007.

[3] S. Kanungo, S. Chattopadhyay, P. Sarathi Gupta, and H. Rahaman, "Comparative performance analysis of the dielectrically modulated full-gate and short-gate tunnel FET-based biosensors," IEEE Trans. Electron Devices, vol. 62, no. 3, pp. 994–1001, Mar. 2015.

[4] R. Narang, M. Saxena, and M. Gupta, "Comparative analysis of dielectric-modulated FET and TFET-based biosensor," IEEE Trans. Nanotechnol., vol. 14, no. 3, pp. 427–435, May 2015.

[5] S. Kanungo, S. Chattopadhyay, P. S. Gupta, K. Sinha, and H. Rahaman, "Study and analysis of the effects of SiGe source and pocket-doped channel on sensing performance of dielectrically modulated tunnel FET-based biosensors," IEEE Trans. Electron Devices, vol. 63, no. 6, pp. 2589–2596, Jun. 2016.

[6] R. Goswami and B. Bhowmick, "Comparative analyses of circular gate TFET and heterojunction TFET for dielectric-modulated labelfree biosensing," IEEE Sensors J., vol. 19, no. 21, pp. 9600–9609, Nov. 2019.

[7] A. Bhattacharyya, M. Chanda, and D. De, "Performance assessment of new dual-pocket vertical heterostructure tunnel FET-based biosensor considering steric hindrance issue," IEEE Trans. Electron Devices, vol. 66, no. 9, pp. 3988–3993, Sep. 2019. [31] TCAD Sentaurus Device User's Manual, Synopsys, Mountain View, CA, USA, 2010.

[8] .R. Purushotham Naik,B. Balaji, A. Krishna Murthy, and E. Radhamma," Design and implementation of low power high-speed CMOS SOI circuit" ISSN: 0094-243X, Volume-2519 Issue-1 Oct, 2022,PP: 050032, https://doi.org/10.1063/5.0120090

[9] . E.Radhamma ,B. Balaji, A. Krishna Murthy, and R. Purushotham Naik," Design analysis and fabrication of FinFET using

3 nm technology" ISSN: 0094-243X, Volume-2519 Issue-1 Oct, 2022,PP: 050033, https://doi.org/10.1063/5.0122967

[10] K. Vennela, B. B, M. C. Chinnaiah and K. Srinivasarao, "Adaptive Backpropagation Algorithm for Clustered Indoor Motion Planning," 2022 2nd International Conference on Intelligent Technologies (CONIT), 2022, pp. 1-4, doi: 10.1109/CONIT55038.2022.9848410.

[11] Balaji, B., Srinivasa Rao, K., Girija Sravani, K. et al. Improved Drain Current Characteristics of HfO2/SiO2 Dual Material Dual Gate Extension on Drain Side-TFET. Silicon (2022). https://doi.org/10.1007/s12633-022-01955-6

[12] Gowthami, Y., Balaji, B. & Rao, K.S. Design and Performance Evaluation of 6nm HEMT with Silicon Sapphire Substrate. Silicon (2022). https://doi.org/10.1007/s12633-022-01900-7

[13] Kumar, P.K., Balaji, B. & Rao, K.S. Performance analysis of sub 10 nm regime source halo symmetric and asymmetric nanowire MOSFET with underlap engineering. Silicon (2022). https://doi.org/10.1007/s12633-022-01747-y

[14] Sravani, S.S., Balaji, B., Rao, K.S. et al. A Qualitative Review on Tunnel Field Effect Transistor- Operation, Advances, and Applications. Silicon (2022). https://doi.org/10.1007/s12633-022-01660-4

[15] Balaji, B., Rao, K.S., Sravani, K.G. et al. Design, Performance Analysis of GaAs/6H-SiC/AlGaN Metal Semiconductor FET in Submicron Technology. Silicon (2022). https://doi.org/10.1007/s12633-021-01545-y

[16] Balaji, B., Rao, K.S., Aditya, M. et al. Device Design, Simulation and Qualitative Analysis of GaAsP/ 6H-SiC/ GaN Metal Semiconductor Field Effect Transistor. Silicon (2022). https://doi.org/10.1007/s12633-022-01665-z

[17] Aditya, M., Rao, K.S., Balaji, B. et al. Comparison of Drain Current Characteristics of Advanced MOSFET Structures - a Review. Silicon (2022). https://doi.org/10.1007/s12633-021-01638-8

[18] Balaji, B., Ajay Nagendra, N., Radhamma, E., Krishna Murthy, A., Lakshmana Kumar, M." Design of efficient 16 bit crc with optimized power and area in vlsi circuits"IJITEE, ISSN: 2278-3075, Volume-8 Issue-8 June, 2019,PP:87-91

[19] Naraiah, R., Balaji, B., Radhamma, E., Udutha, R." Delay approximation model for prime speed interconnects in current mode"IJITEE, ISSN: 2278-3075, Volume-8 Issue-9, July 2019,PP:3090-3093

[20] Sudhakar Alluri,K. Mounika,B.Balaji. , D.Mamatha," A Novel Implementation of 4 Bit Parity Generator in 7nm Technology" ISSN: 0094-243X, Volume-2358 Issue-1 July, 2021,PP: 030002- 1-10 , https://doi.org/10.1063/5.0059329

[21] Sudhakar Alluri, B.Balaji,Ch.cury" Low power, high speed VLSI circuits in 16nm technology" ISSN: 0094-243X, Volume-2358 Issue-1 July, 2021,PP: 030001- 1-16 , https://doi.org/10.1063/5.0060101

[22] Sudhakar Alluri,K. Mounika,B.Balaji. , D.Mamatha," Optimization of multiplexer architecture in VLSI circuits" ISSN: 0094-243X, Volume-2358 Issue-1 July, 2021,PP: 040004- 1-19 , https://doi.org/10.1063/5.0059332

[23] P. Ashok Kumar, K. Srinivasa Rao, K. Girija Sravani, B. Balaji, M. Aditya, Koushik Guha, Ameen Elsinawi,"An intensive approach to optimize capacitive type RF MEMS shunt switch",Microelectronics Journal,Volume 112,2021,105050,ISSN 0026-2692, https://doi.org/10.1016/j.mejo.2021.105050.

[24] Sravani, K.G., Guha, K., Aditya, M. et al. "Design, simulation and analysis of uniform and non-uniform serpentine step structure RF MEMS switch(2021). https://doi.org/10.1007/s00542-021-05216-1

[25] Kumar, P.A., Rao, K.S., Balaji, B. et al. "Low Pull-in-Voltage RF-MEMS Shunt Switch for 5G Millimeter Wave Applications". Trans. Electr. Electron. Mater. (2021). https://doi.org/10.1007/s42341-021-00304-5

[26] Aditya M, I Veeraraghava Rao, B. Balaji, John Philip B, Ajay Nagendra N, S Vamsee Krishna." A "IJITEE, ISSN: 2278-3075, Volume-8 Issue-7 May, 2019,PP:217-220

[27] Balaji, B., Aditya, M., Adithya, G.Ayyappa Vijay, V.V.S.S.K., Chandu, K." Implementation of low-power 1-bit hybrid full adder with reduced area"IJITEE, ISSN: 2278-3075, Volume-8 Issue-7, 2019,PP:61-64

[28] Chokkara, S.P., Gaur, A., Sravani, K.G. et al. Design, Simulation and Analysis of a Slotted RF MEMS Switch. Trans. Electr. Electron. Mater. (2021). https://doi.org/10.1007/s42341-021-00363-8,24.09.21

[29] Soma, U., Suresh, E., Balaji, B., Ramadevi, B. (2023). Device Design and Modeling of Fin Field Effect Transistor for Low Power Applications. In: Satapathy, S.C., Lin, J.CW., Wee, L.K., Bhateja, V., Rajesh, T.M. (eds) Computer Communication, Networking and IoT. Lecture Notes in Networks and Systems, vol 459. Springer, Singapore. https://doi.org/10.1007/978-981-19-1976-3_45

[30] Gowthami, Y., Balaji, B. & Rao, K.S. Design and Analysis of a Symmetrical Low-κ Source-Side Spacer Multi-gate Nanowire Device. J. Electron. Mater. (2023). https://doi.org/10.1007/s11664-023-10217-z