Scalable low-power 1-bit hybrid full adder for fast computation using Pass Transistors.

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Abstract
Using pass transistor logic, we constructed a 1-bit full adder circuit in this study. High-speed technology uses pass transistor logic, and it is simple to construct the fundamental gate architectures. An improvement on the pass transistor logic Ex-or gate is the designed circuit. The I-V characteristics and power for sum and carry were computed for the 1-bit Full Adder Circuit. The performance assessment of a 1-bit full adder circuit allows for the analysis of the impact of scaling on overall performance. In order to compare the functionality of the proposed full adder circuit with the conventional design and to ensure its efficacy, simulations have been performed on the LT Spice tool simulator at 1.8v single ended supply voltage. The results show that the circuit has low power dissipation at high speeds.

Key: Scalable, low-power, 1-bit, hybrid, full adder, fast computation,Pass Transistors.

INTRODUCTION

A digital circuit that performs addition is called a full adder. Hardware implements full adders us ing logic gates. Three one-bit binary values, two operands, and a carry bit are added using a com plete adder. Two numbers are produced by the adder: a sum and a carry bit. When compared to a half adder, which adds two binary digits, the term is used. Two binary values and a carry or overf low bit are required by a complete adder. An additional carry bit and a total are the outputs. Hard ware XOR, AND, and OR gates are used to build full adders. To add bits to any number of bits, s uch as 32 or 64 bits, full adders are frequently coupled to one another. An XOR and a full adder are equivalent to two half adders.

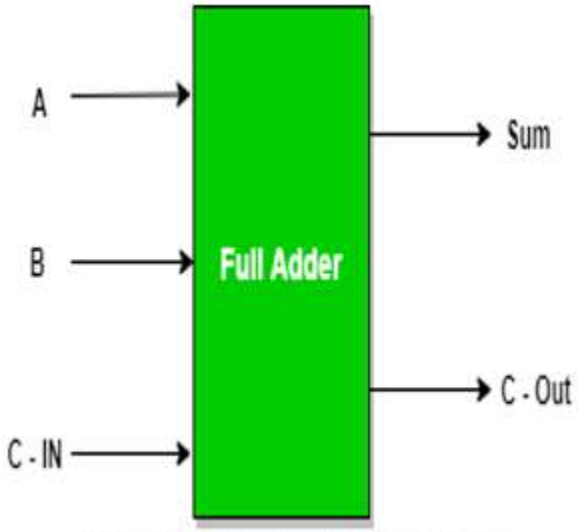

Fig. 1 Block diagram of Full Adder Circuit

The adder known as a "full adder" adds three inputs and generates two outputs. A and B make up the first two inputs, while C-IN is the third input. The normal output is denoted as S, which represents SUM, while the output carry is designated as C-OUT. Eight inputs can be used to form a byte-wide adder using full adder logic, and the carry bit can be cascaded from one adder to the next. We employ a complete adder since a 1-bit half-adder cannot use a carry-in bit when one is available, therefore we must use another 1-bit adder. Three operands are added via a 1-bit complete adder, which produces 2-bit output.

IMPLEMENTATION

Pass Transistor Logic

Pass transistor logic (PTL) in electronics refers to a number of logic families utilised in the creation of integrated circuits. By removing unnecessary transistors, it lowers the number of transistors needed to create various logic gates. Instead of switches linked directly to supply voltages, transistors are employed as switches to transmit logic levels between circuit nodes. While this minimises the number of active devices, it has the drawback of causing the voltage difference between high and low logic levels to narrow with time. At its output than at its input, each transistor in a series configuration is less saturated. It could be necessary to use a gate with a typical construction to restore the signal voltage to its original value if many devices are coupled in series in a logic circuit. Conventional CMOS logic, in contrast, switches transistors such that the output links to one of the power supply rails (similar to an open collector method), maintaining the logic voltage levels in a sequential chain. It can be necessary to simulate circuits to guarantee acceptable performance.

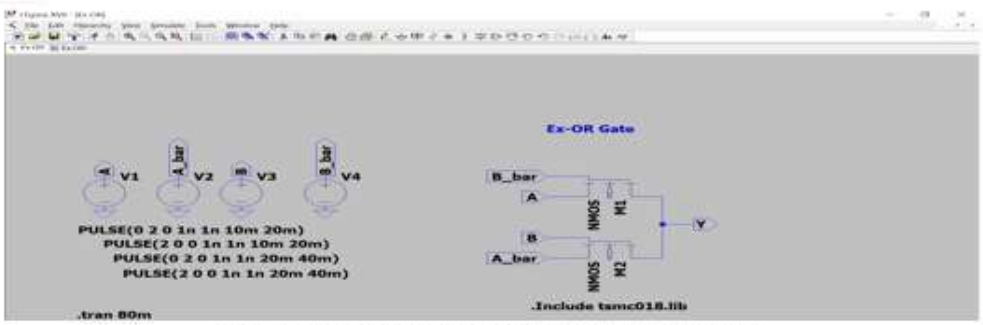

Fig. 2 Ex-or gate circuit diagram using Pass Transistor Logic

Fig.2 represents the circuit diagram of the Ex-or gate with pass transistor logic with all the inputs and outputs applied in LT Spice tools.

Fig. 3 Ex-or gate output

The Results obtained from the Ex-or gate using Pass Transistor Logic and is observed and verified with the truth table and is shown in Fig. 3.

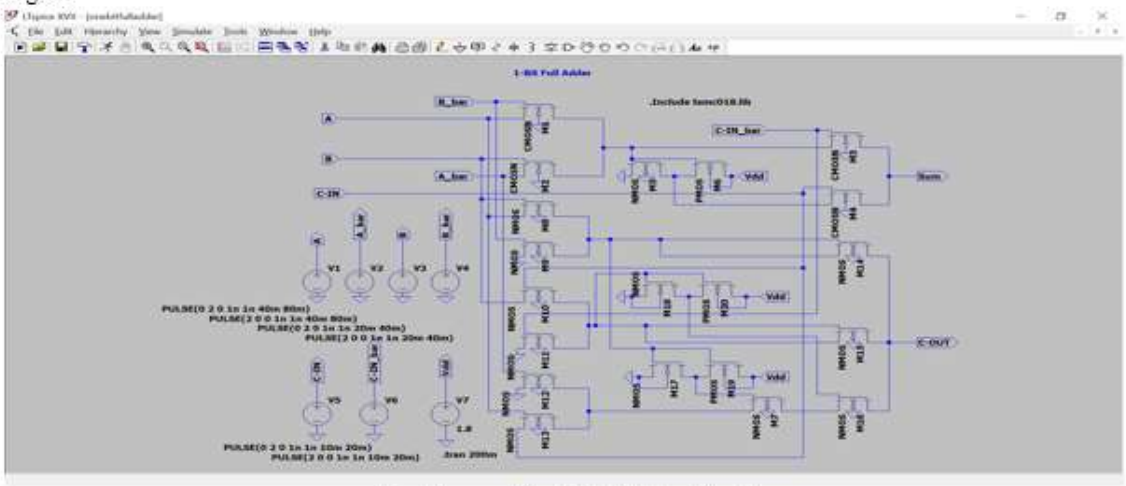

Fig. 4 Proposed One-bit Full Adder Circuit

Applications

When compared to fully complementary CMOS logic, pass transistor logic frequently utilises fewer transistors, performs the same operation quicker, and uses less power. If implemented using only basic gates, XOR has the worst-case Karnaugh map and uses the most transistors of

all the operations. By adopting pass-transistor logic rather than basic gates to construct the XOR, the designers of the Z80 and several other devices were able to save a few transistors.

Basic Principles Of Pass Transistor Circuits

A periodic clock signal drives the pass transistor, which functions as an access switch to charge or discharge the parasitic capacitance Cx based on the input signal Vin. Thus, two potential operations are the logic "1" transfer (charging the capacitance Cx to a logic-high level) and the logic "0" transfer (charging the capacitance Cx to a logic-low level) while the clock signal is active (CK = 1). Regardless of the voltage Vx, the output of the depletion load nMOS inverter plainly takes on a logic-low or a logic-high state.

Fig. 4 represents the proposed circuit diagram of Implemented one bit Full Adder Circuit with Pass Transistor Logic with all the inputs and outputs applied in LT Spice tools.

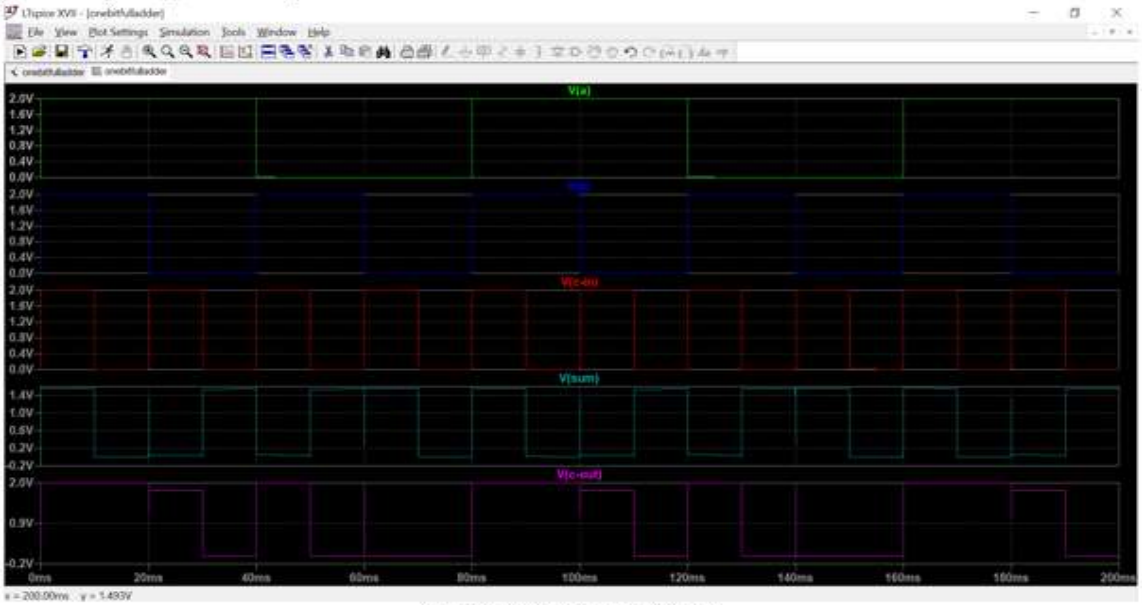

Fig. 5 One-bit Full Adder Outputs

Fig. 5 shows the obtained results from the Full Adder circuit using pass transistor logic is observed and verified with the truth table.

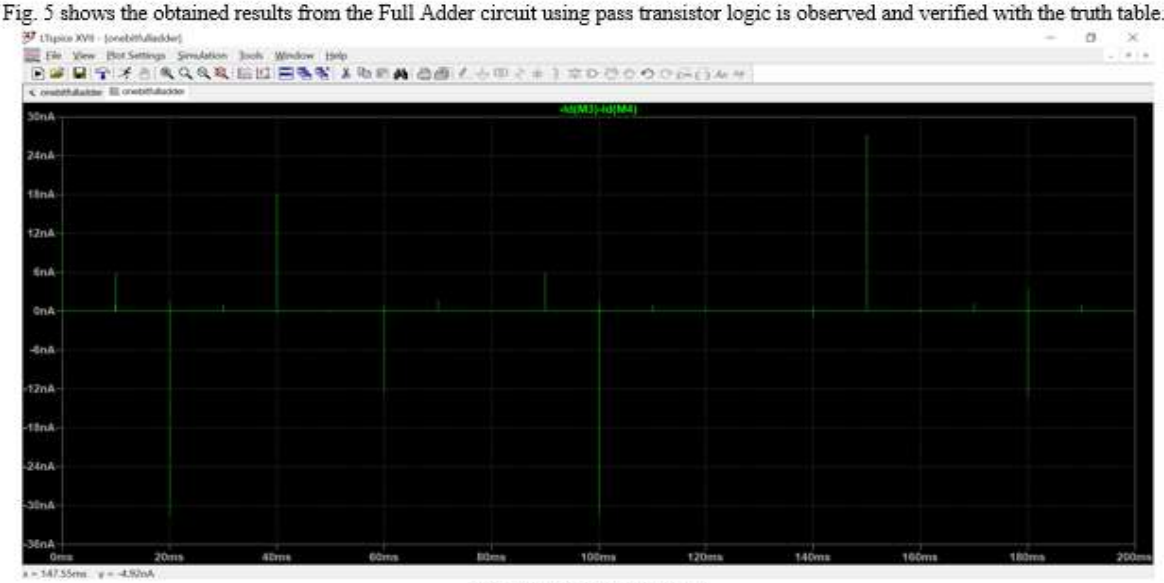

Fig. 6 Sum output current

Complementary Pass Transistor Logic

A method of creating logic gates that employs transmission gates made of both nMOS and pMOS pass transistors is referred to as "complementary pass transistor logic" by certain writers.

Other publications refer to a certain method of creating logic gates as "complementary pass transistor logic" (CPL), where each gate is made up of a nMOS-only pass transistor network followed by a CMOS output inverter. Other writers refer to a method of creating logic gates utilising dual-rail encoding as "complementary pass transistor logic" (CPL). Since each CPL gate has two output wires, one for the positive signal and the other for the complementary signal, inverters are not required.

Logic family known as "Differential pass transistor logic" or "Complementary pass transistor logic" is created with a specific benefit. For multiplexers and latches, this logic family is frequently used. To choose amongst potential inverted output values of the logic, which drives an inverter, CPL employs series transistors. NMOS and pMOS transistors are linked in parallel to form the CMOS transmission gates.

RESULTS

There are two forms of pass transistor logic: static and dynamic, with varying characteristics in terms of speed, power, and low-voltage operation. The drawbacks of pass transistor logic become more pronounced when the supply voltages for integrated circuits drop; the threshold voltage of transistors rises above the supply voltage, drastically reducing the number of consecutive steps. Additional logic stages are needed to regulate pass transistors since complementary inputs are frequently needed. Pass transistor logic is used to create the circuit, and the Ex-or gate circuit was initially built with the use of this logic. and flawlessly observed the outcome. Tested by applying voltages of 1.8 and 2 volts, and the simulation results are checked against a truth table.

Conclusion

The simulation results have demonstrated the 1-bit Full Adder Circuit's proper operation, and this work has provided a brief description of its architecture utilising pass transistor logic. By optimising the values of the drain and source voltages, the output voltage values of C-OUT may be lowered to the logic values of other signals. In comparison to the current complete adder circuit models, the constructed Sum and C-OUT circuits are anticipated to perform better and use less power. Our suggested design has significantly reduced space, voltages, currents, and power; nevertheless, these factors can still be improved upon. In comparison to the current adders, very little distortion has been seen. The implemented architecture is utilised to create 16-bit and 32-bit adders as well as for future analysis, however the aim of this implementation was to design the ALU's sub-blocks.

References

[1] Lee Shing Jie and Siti Hawa Ruslan, “A 4-bit CMOS Full Adder of 1-bit Hybrid 13T Adder With A New SUM Circuit”, 2016 IEEE Student Conference on Research and Development (SCOReD). 2022.

[2] Jyoti Rani and Atul Kumar Nishad, "A Novel Approach to Design Low Power and HighSpeed Self-Repairing Full Adder Circuit", Proceedings of the Second International Conference on Intelligent Computing and Control Systems (ICICCS 2018), pp.1938-1942.
[3] Phanindra L S, Rajath M N, Rakesh V, Vasundara Patel K S, " A Novel Design and Implementation of Multi-Valued Logic Arithmetic Full Adder circuit using CNTFET", IEEE International Conference On Recent Trends In Electronics Information Communication Technology, May 20-21, 2021, India. Pp 563-568.
[4] Chaitali P. Kadu and Manish Sharma, "Area-Efficient High-Speed Hybrid 1-bit Full Adder Circuit Using Modified XNOR Gate", IEEE, International conference on Information, Communication, Instrumentation and control, 2020.
[5] S. M. Ishraqul Huq, Maskura Nafreen, Tasnim Rahman and Sushovan Bhadra, "Comparative Study of Full Adder Circuit with 32nm MOSFET, DG-FinFET and CNTFET", Proceedings of the 2017 4th International Conference on Advances in Electrical Engineering. Pp 38 -43.
[6] Sri Harsha Bandarupalli, Bala Pavan Kalyan Bandi, Rahul Kumar Reddy Boggula, Kirti S. Pande "Compressor Using Full Swing XOR Logic Gate", IEEE, pp. 84-89.
[7] Ishika Sharma and Rajesh Mehra, "Delay Analysis of Half Subtractor using CMOS and Pass Transistor Logic", International Journal of Computer Applications (0975 – 8887) Volume 141 – No.12, May 2016.
[8] Sathaporn Lueangsongchai and Siraphop Tooprakai, "Design high speed and low power hybrid full adder Circuit", The 18th International Symposium on Communications and Information Technologies (ISCIT 2018), pp 22-25.
[9] Mandar Gadekar, Rajiv Chavan and Nikhil Matkar, "Design of 16T Full Adder Circuit Using 6T XNOR Gates" 2017 IEEE, 2017.
[10] Muyu Yang and Erdal Oruklu "Full Adder Circuit Design Using Lateral Gate-All-Around (LGAA) FETs Based on BSIM-CMG Model", 2018 IEEE, 2018. Pp.420-423.

[11] Sarada Musala and B. Rajasekhara Reddy, "Implementation of a Full Adder Circuit with New Full Swing Ex-OR/Ex-NOR Gate", 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), pp 29-33.

[12] Jiwanjot Kahlon, Pradeep Kumar and Anubhav Garg, Ashutosh Gupta, "Low Power and Temperature compatible FinFET based Full Adder circuit with optimised Area", 2016 Intl. Conference on Advances in Computing, Communications and Informatics (ICACCI), Sept. 21-24, 2016, Jaipur, India.pp-2121-2125.

[13] Ashish Yadav, Bhawna P. Shrivastava and Ajay Kumar Dadoria, "Low Power High Speed 1-bit Full Adder Circuit Design in DSM Technology", IEEE International Conference on Information, Communication, Instrumentation and Control (ICICIC-2017).