A LOW AREA AND DELAY EFFICIENT DESIGN OF 5-2 COMPRESSOR

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Abstract- Compressors are the fundamental components in the partial product reduction stage of CMOS multipliers. A new design is presented for the CMOS 5-2 compressor with 58 transistors, which is the lowest reported device count for such a circuit. Simulation results show that the proposed 5-2 compressor has significantly improved power-delay performance compared to previously proposed approaches. The overall design is performed in DSCH and Microwind 65nm technology and individual block is examined before designing the 5-2 compressor.

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I. INTRODUCTION

Multiplication is a very common and important operation in general purpose microprocessors and digital signal processors. Its speed is often a determining factor of how fast the processors can operate. A fast multiplication process usually uses an array multiplier and consists of three stages: partial product generation, partial product reduction and final carry-propagating addition. In large multipliers, the second stage usually contributes the most in delay, power and area, therefore improvement in this field is deemed essential.

The partial product reduction can be efficiently implemented with compressor trees, which commonly use 4-2 and 5-2 compressors as building blocks. Improving the compressor cell directly affects the overall performance of the multiplier. A 5-2 compressor was initially used in for the design of a high performance 16 × 16-bit multiplier, however specific transistor-level implementation was not provided we propose a new low-power and high-performance CMOS 5-2 compressor with a low transistor count. A comparative study is also conducted to evaluate the new circuit against prior works.

A. Application of Compressors

B. 5-2 Compressor functionality

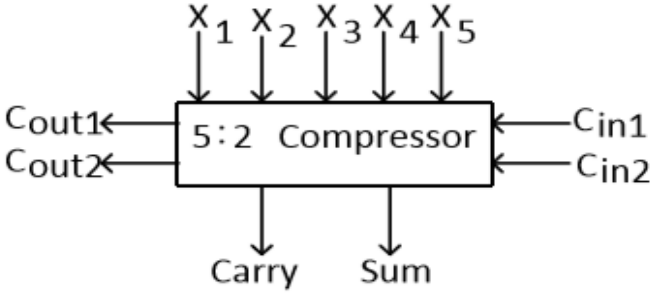

Fig.1 Basic 5:2 compressor design

The 5-2 compressor receives seven inputs of equal weight, including five primary inputs $X_{1–5}$ and two inputs Cin_{1-2} that receive their values from the neighboring compressor of 1 binary bit order lower It generates an output *Sum* of the same weight as the inputs and three outputs $Cout_{1-2}$, *Carry* weighted 1 binary bit order higher. Its functionality is described by the following binary arithmetic equation:

$$X_1 + X_2 + X_3 + X_4 + X_5 + Cin_1 + Cin_2 = Sum + 2 \times (Cout_1 + Cout_2 + Carry) \quad (1)$$

Fig. 1 shows a conventional implementation of the 5-2 compressor using a cascade of three full adders. In its general form, a full adder receives three inputs (a, b, c) and generates two outputs (S_{FA}, C_{FA}), which can be the following Boolean equations

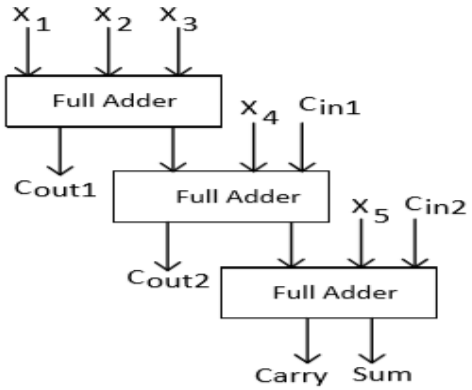

Fig.2. 5: 2 compressor with full adders

$$S_{FA} = a \wedge b \wedge c \quad (2)$$

$$C_{FA} = (a \wedge b) \cdot c + (a \wedge b)' \cdot a \quad (3)$$

Consecutively, by applying (2) and (3) to the 5-2 compressor of Fig. 1, we obtain the following set of Boolean equations:

$$Sum = X_1 \wedge X_2 \wedge X_3 \wedge X_4 \wedge X_5 \wedge Cin_1 \wedge Cin_2 \quad (4)$$

$$Cout_1 = (X_1 \wedge X_2) \cdot X_3 + (X_1 \wedge X_2)' \cdot X_1 \quad (5)$$

Cout2=(x1^x2^x36x4).cin+(x1^x2^x3^x4)'.x4 (6)

Carry=(x1^x2^x3^x4^x5^cin).cin2+(x1^x2^x3^x4^x5^cin1)'.x5 (7)

II. CONVENTIONAL 5-2 COMPRESSOR

A. 5-2 conventional compressor:

This conventional implementation is not very efficient, since it has a critical path of six gate delays for the *Sum* and *Carry* outputs. Several alternative architectures have been proposed, using fewer logic stages and in some cases producing output equations that differ from (4)–(7). Nonetheless, all designs must abide by (1) for valid operation.

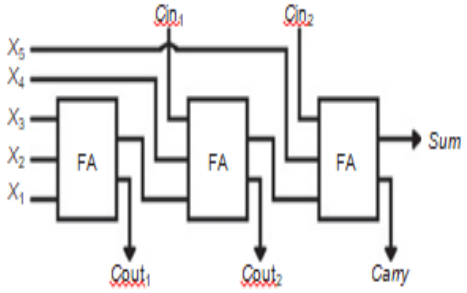

Fig.3 *Conventional implementation of 5-2 compressor with full adders*

B. Disadvantage of conventional 5-2 compressor

It is not very efficient, since it has a critical path of six gate delays for sum and carry output. In order to overcome this problem we design 5-2 compressor using CMOS logic

C. Overview

Higher order multiplication, a huge number of adders or compressors is to be used to perform the partial product addition. We can reduce the number of adders by introducing special kind of adders that area capable of add five/six/seven bits per decade these adders are called compressors

III. PROPOSED COMPRESSOR

A. New 5-2 compressor

We propose a new low-power and high-performance CMOS 5-2 compressor with a low transistor count. A comparative study is also conducted to evaluate the new circuit against prior works. A new design is presented for the CMOS 5-2 compressor with 58 transistors, which is the lowest reported device count for such a circuit.

B. Proposed circuit

A block diagram of the proposed 5-2 compressor is shown in Fig. *a*. It consists of six XOR and three MUX blocks, whose generalised schematics are shown in Figs. *b* and *c*, respectively. This compressor is characterised by (4)–(7), similar to the conventional one. The functionality of the full adder was decomposed into two XOR gates and a 2-1 MUX and these basic cells were rearranged to achieve a smaller critical path. Consequently, this structure requires four gate delays to produce the *Sum* and *Carry* outputs.

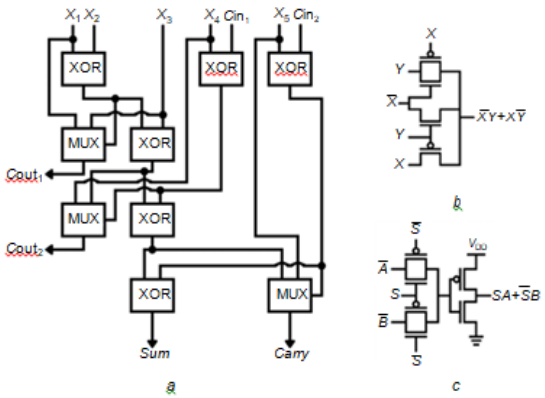

Fig.4 Architecture of the proposed 5-2 compress*a* Block diagram
b Schematic of 2-input XOR cell
C Schematic of 2-1 MUX cell

The complete transistor-level schematic of the proposed 5-2 compressor is shown in Fig. 5. It uses full-swing transmission gate logic and static inverters so that no threshold drops occur in intermediate nodes and output nodes are fully restored. These traits make it suitable for

voltage/process scaling and cascading. Furthermore, unlike previous designs, this one completely avoids the use of complex static CMOS gates and dual rail XOR-XNOR logic, which require more transistors for their implementation

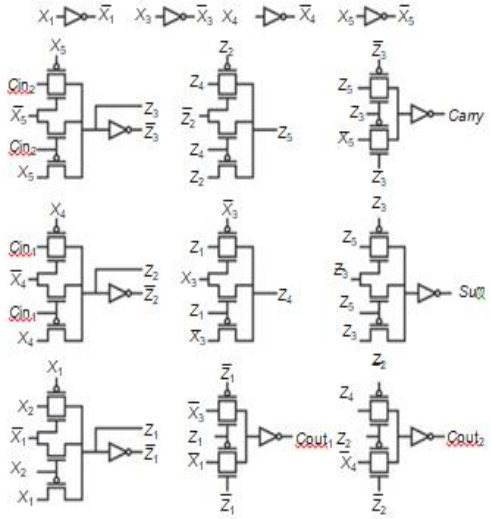

Fig. 5 Transistor level implementation of the proposed 5-2 compressor

C. OVERVIEW

Compressors are the fundamental components in the partial product reduction stage of CMOS multipliers. A new design is presented for the CMOS 5-2 compressor with 58 transistors, which is the lowest reported device count for such a circuit and it overcome the critical path delay occurred due to six gate for sum and carry output in conventional 5-2 compressor. The proposed 5-2 compressor has significantly improved power-delay performance compared to previously proposed approaches.

IV. SIMULATION RESULTS AND COMPARISION

The proposed low power high-performance CMOS 5-2 comparator with 58 Transistors the circuits were designed using 65nm CMOS process in MICROWIND, the size of PMOS is triple that of the NMOS transistor size to achieve the best power and delay performance. The simulations were done using DSCH and MICROWIND with a power supply of 1V. Simulation result and digital schematic of some of the circuits using DSCH 3.5 tool are given below.

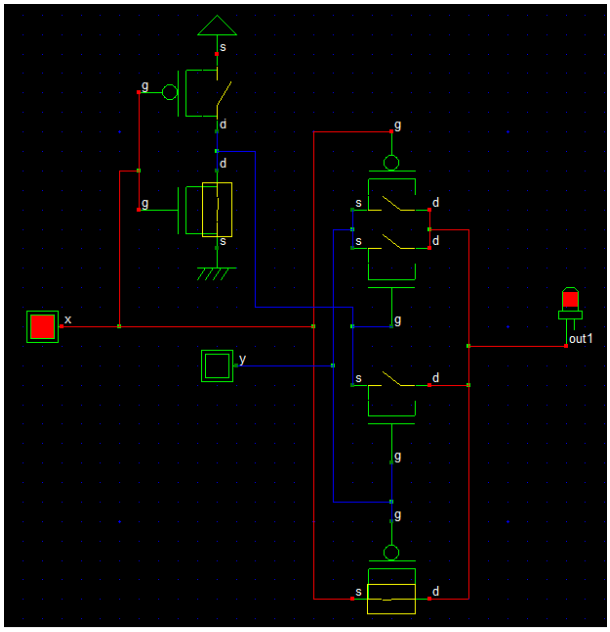

Fig 6.1. Schematic of 2 input XOR cell in DSCH

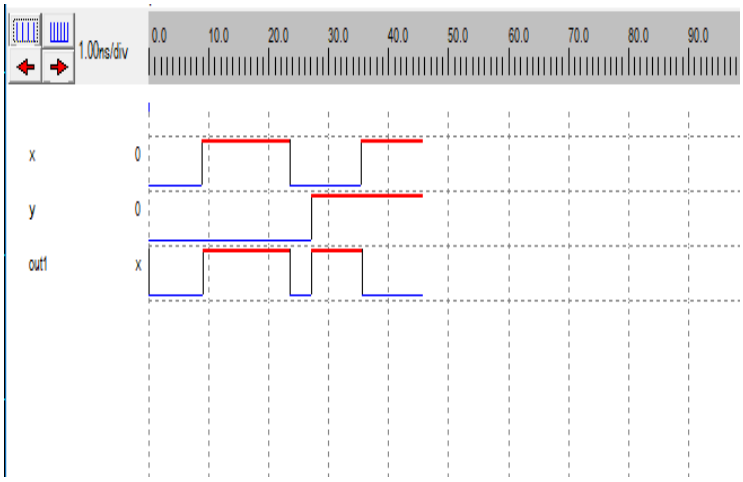

Fig 6.2. Simulation result of 2 input XOR cell in DSCH

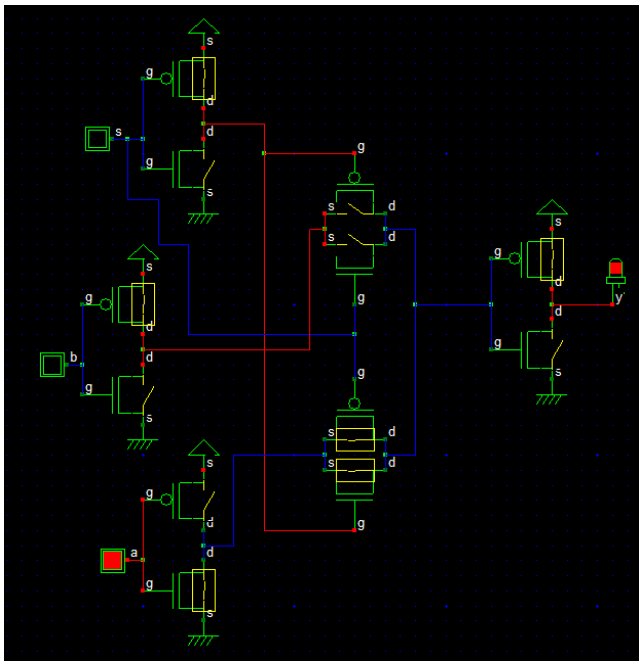

Fig. 6.3 schematic of 2x1 mux in DSCH

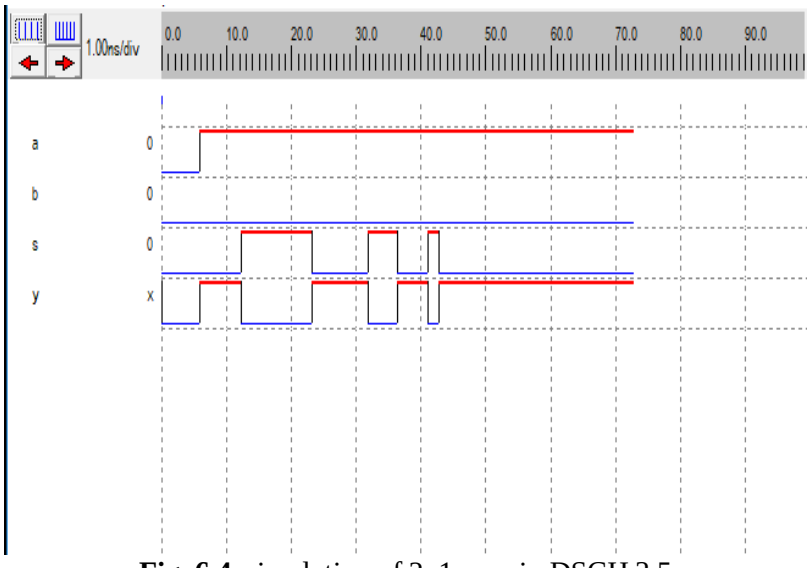

Fig .6.4 simulation of 2x1 mux in DSCH 3.5

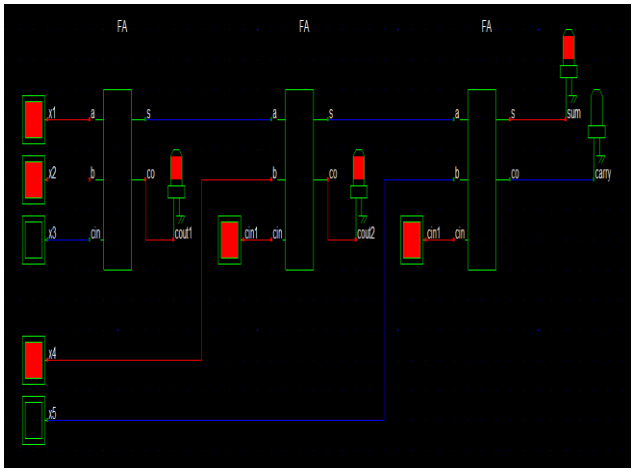

Fig6.5. Schematic of conventional 5-2 compressor with full adders

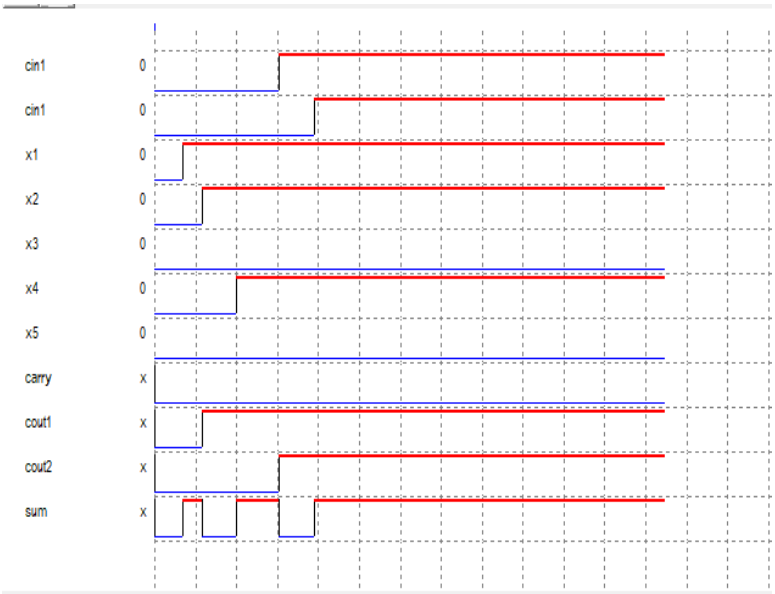

Fig 6.6. Simulation of conventional 5-2 compressor in DSCH

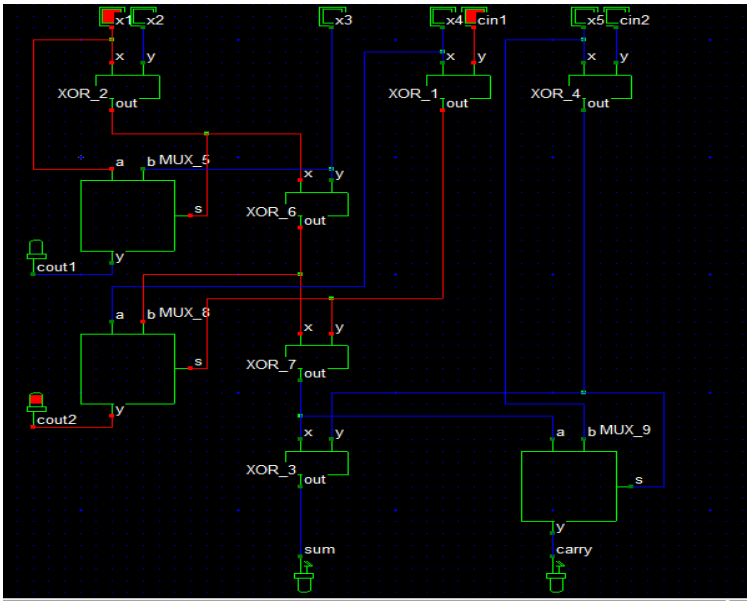

Fig 6.7.schematic of proposed 5-2 compressor in DSCH 3.5

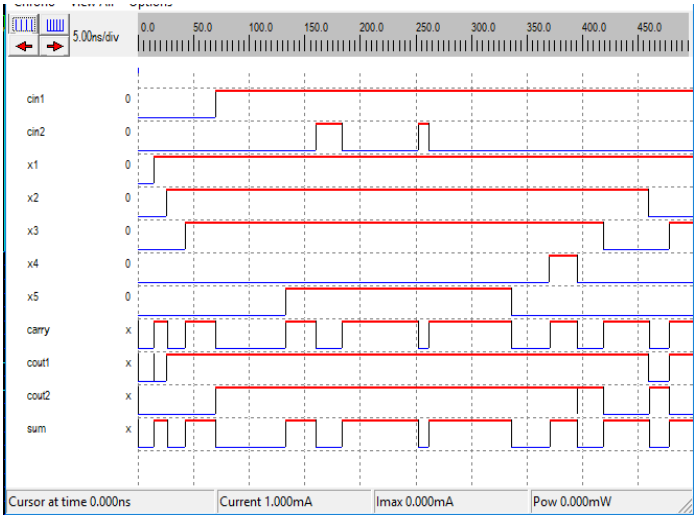

Fig 6.8. Simulation of proposed 5-2 compressor in DSCH

The Verilog files which are generated in DSCH are compiled in MICROWIND 3.5 and is implemented on CMOS 65 nm technology, from which we can calculate the power and number of transistors used to design the proposed circuit and can be compared with the existing design in terms of power and area and count of transistor.

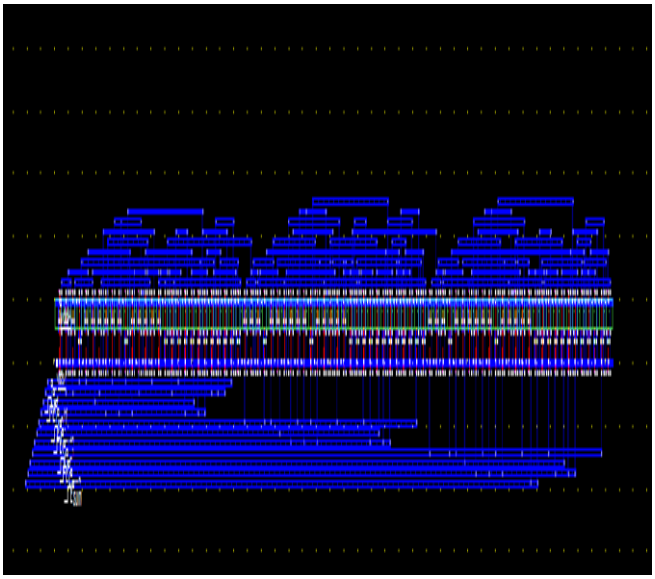

Fig 6.9: layout of conventional 5-2 compressor on 65 nm technology CMOS technology using MICROWIND 3.5 tool

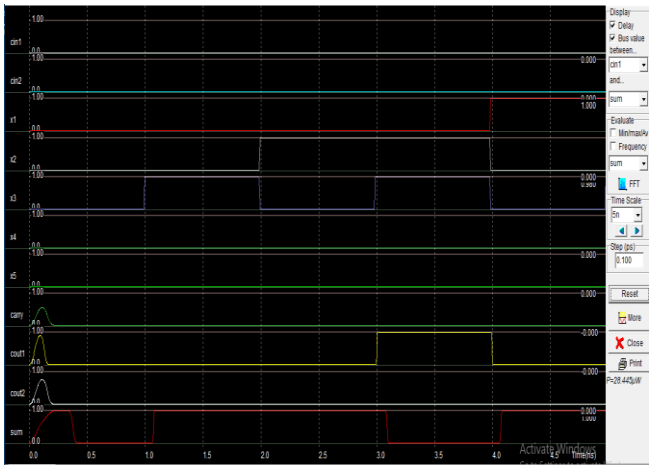

Fig 6.10 waveform of conventional 5-2 compressor

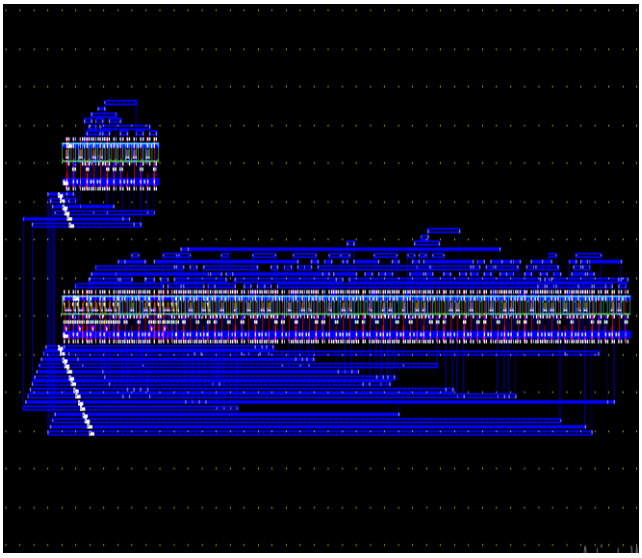

Fig 6.11. Layout of proposed 5-2 compressor implemented on 65nm CMOS technology

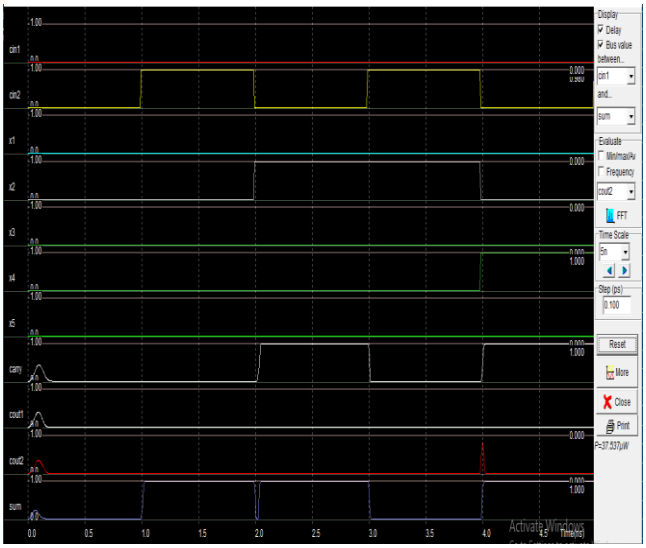

Fig 6.12 waveform proposed 5-2 compressor of

Table 1: Comparison of 5-2 compressors

Design		Transistors	Power
Existing [6]		**94**	**76.302µw**
Existing [8]		**78**	**54.452µw**
proposed		**58**	**37.537µw**

According to Table 1, the proposed 5-2 compressor has the lowest transistor count, achieving 23.6–38.3% improvement compared to [6–8]. Furthermore, it has the lowest power dissipation compared to pre-layout simulation

V. CONCLUSION

We presented a new design for the CMOS 5-2 compressor which has the lowest reported device count of 58 transistors. The pro- posed circuit uses full-swing logic with fully restored outputs and is thus suitable for process scaling and cascading. Furthermore, according to the simulation results, it achieves the best overall power–delay performance compared to previously proposed designs. It is concluded that the new 5-2 compressor can be utilized as an efficient component of low-power and high-performance CMOS multipliers.

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