Design and Implementation of an XOR Based 16-bit Carry Select Adder for Area, Delay and Power Minimization

Dr. Nookala Venu

Assistant Professor, Internet of Things (IoT), Offered by Department of IT, Madhav Institute of Technology & Science, Gwalior - 474 005, Madhya Pradesh, India, (A Govt. Aided UGC Autonomous Institute).

venunookala@mitsgwalior.in

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Abstract

In different types of processors and other digital circuits adders are most widely used. Low power and area efficient high-speed circuits are most substantial area in the research of VLSI design. The carry select adder is one of the fast adders which has less area and reduced power consumption. In this paper, a 16-bit carry select adder has been presented using modified XOR based full adder to reduce circuit complexity, area and delay. The modified full adder design requires only two XOR gates and one multiplexer. The modified 16-bit carry select adder gives better result than conventional carry select adder with respect to area, power consumption and delay.

Keywords: *Low Power, Area Efficient, XOR based Adder, Carry select Adder.*

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1. Introduction

In digital integrated circuit design, addition is the heart of computer arithmetic. It has special significance in processors and many other digital circuits. In rapidly growing mobile industry faster units, smaller area and less power become major concern. For increasing portability of mobile electronics, area and power are the key factors [1-2]. They also major concern to increase battery life. In VLSI system, reduction in area and power are the main focus point of research. Faster speed for addition and multiplication is a fundamental requirement of high-performance processors. Arithmetic units are the work horse of a computational circuit and addition is the heart of this. In VLSI sub system the power efficient and high-performance adders are most desired digital circuit. Speed of adder is usually limited for carry propagation bit. The sum of each bit in an adder is generated sequentially after the addition of previous bit and a carry propagated to the next position [3-4]. There are plenty of adder designs available

in the literature such as Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Select Adder (CSA), Carry Skip Adder which have their own advantages and disadvantages. CSA is one of the fastest adders because of its less area and power consumption. In CSA there are two multiplexed RCA which act in parallel assuming carry in, Cin = 0 and in other Cin = 1, then final sum is selected through multiplexer [5-8]. In conventional CSA, XOR, AND and OR gate based full adders are used. These adders consumes more area in the chip due to large number of transistors are used in these gates, the delay is higher and consumes more power. In the present work, XOR based modified full adder have been used as the building blocks of the modified CSA to reduce area, delay and power consumption. The layout of the 16-bit CSA is designed in Micro wind software [9-14]. The results obtained from the layout data is compared with the conventional CSA. In digital integrated circuit design, adders are among the most common building blocks of microprocessor processors. You can't have DSP programmes without them. Researchers have attempted, and continue to attempt, to create adders that provide fast speed, low power consumption, reduced area, or some combination of these benefits as technology progresses. There is a carry value that is produced by each adder in an arithmetic sequence and must be passed on to the next adder in the sequence. As a result, this significantly lengthens the circuit's critical route delay [15-23]. There is less delay in the circuit if the carry is propagated across fewer stages. The necessary total is determined using a multiplexer. Adders can be treated as building blocks of the arithmetic component. For the operations like complementing, decoding and encoding adders are used. Generally, addition involves adding of two numbers which generates sum and carry. All adder architectures either simple or complex are constructed by using fundamental blocks which are half adder and full adder. For small number of bits, simple adders like ripple carry adder, carry look ahead adders are sufficient [24-29]. However, delay increases as the bits number increases because of the passing of the carry to the next stage. So, we use Parallel Prefix Adders to perform arithmetic operations on large number of bits. Parallel prefix adders are high speed adders and take small area and give less delay. These adders consume low power and relatively take less area on chip. Primary concern of adders is speed and later we have chip area and power consumption of adder [30-34].

2. Literature Review

FPGAs are susceptible to soft errors (SEs), although there are ways to protect against or identify them. Data cleaning is one example (DS) Scanning the entire device's memory at regular intervals to fix any problems found is the essence of DS. To replace the corrupted frames, you need to save the original configuration data or at least a portion of it. However,

as ECC codes can only correct a single bit or two neighboring bits in a frame, including ECC bits in every frame of the FPGA bit stream may not be enough [35-41]. Bit stream security is provided by both ECC and cyclic redundancy check (CRC) codes; however the latter are only effective for integrity checks and not error repair. Another popular approach to improving dependability and spotting SEs is the use of triple module redundancy (TMR) in conjunction with a voter mechanism. Even though this technique greatly extends the MTTF, it also triples the area and power requirements compared to the pioneering design [42-48]. The snake is an essential element in every modern area. In this digital age, everyone is working on miniaturization. The three main aspects of design, namely, area, power consumption and delay need to achieve optimal balance. Because helpers have been used as a key component of complex digital networks, increasing the performance of digital providers will accelerate the speed of binary operations in such complex zones [49-54].

A good VLSI model is a design with small footprints and quick surgery. According to Moore's law, as the number of transistors in a chip increases, so does the overall chip area. In VLSI design, it is important to improve the Area and Delay parameters. The field of Very Large-Scale Integration (VLSI) design; circuit summing is one of the most widely used data transmission architectures [55-59]. With the advancement of VLSI technology, research is emerging to design low-speed, high-speed, small-area, or combination of two architectures. The design of ads implemented through memristor. Explains the memristor-based design for standard ad architectures (ripple-bearing adder, bearing adder, and corresponding prefinder adder). Compare area and waiting time [60-63]. Surprisingly, the Radix-2 CLA has the same complexity as the parallel adder prefect. The results show that in the adjacent price adder, the Kogge-Stone design has the best metrics for latency and area. An effective insect repellent design, which uses a multiplexer-based multiplexer design rather than using a snake-bearing wound, but an improved enhancer Replace the ripple bearing snake for effective results. Using this improved snake can reduce power consumption and reduce gate delays [64-68]. The proposed proposal is to carry and store oil from 8-bit to 64-bit. With today’s digital technology system, which is the most widely used 64-bit format? Since ripple-carrying snakes are one of the most common types of auxiliaries used in many forms, there is a prolonged delay in propagation and consuming more area and energy. Single-bit full-adders are cascaded for construction of the ripple carry adder [69-74]. Each full-adder prior carrying-out signals is ready in the RCA, then only begins its computation. In a carrying ripple adder, the carry-out propagation direction, therefore, specifies the critical path delay. As shown in Figure 1, for a full-adder N-bit, the essential paths in the full-adders are N-bit

carrying propagation paths. The delay time in the N- bit RCA increases linearly as the N-bit increases [75-78].

All modern processors, including microprocessors and digital signal processors, have an arithmetic logic unit (ALU). The computational performance of these modern processors depends on the success of the ALU. The serpent is the foundation stone of the ALU which performs arithmetic and logical work [79-80]. Existing helpers (such as half helpers, full helpers, ripple converters, skip carry assistants and pre-loaders) cannot respond to improvement goals, so this paper offers four types of introductions. Evaluates the decrease in conventional power consumption by lending collectors - money at low voltage and analyses the effects of the difference between the effectiveness of the ripple bear adder (RCA) and the adder te-save-adder (BSA). A higher rate of deferral and the provision of technological means to enhance the BSA's adaptability to change [81-82]. In addition to discussing the effectiveness of power reduction in snakes, this article also delves into the concept of so-called pipelines and the typical methods used to obtain currency.

3. Description of the Proposed Scheme

3.1 XOR Based Full Adder

A full adder which is the main building block of n-bit adders gives the result of addition with output carry taking input carry in to consideration. So, actually a one-bit full adder adds three one-bit numbers A, B, and Cin where A and B are the operands, and Cin is a bit carried in from the previous less-significant stage. A conventional full adder implementation based on basic logic gates is shown in Fig. 1.

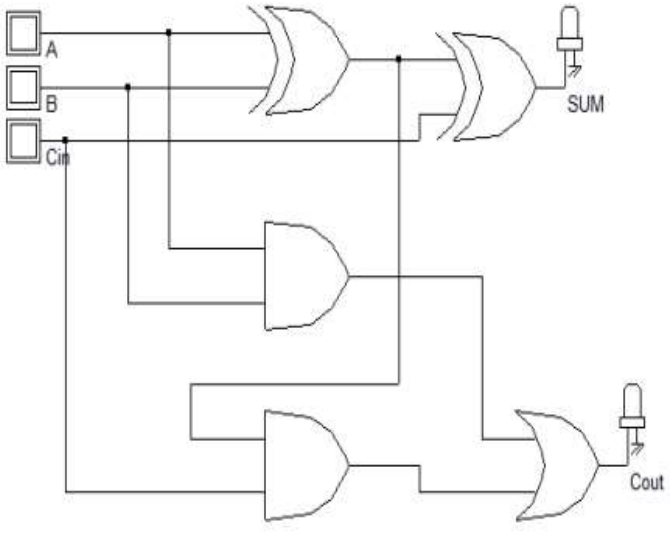

Fig.1: Conventional 1-bit full adder

A binary full adder realization employing two XOR gates and one 2:1 MUX is shown in Fig. 2. The layout of conventional and XOR based 1-bit full adder are shown in Fig. 3 and Fig. 4 respectively. The advantage of XOR based adder is that it requires smaller number of transistors.

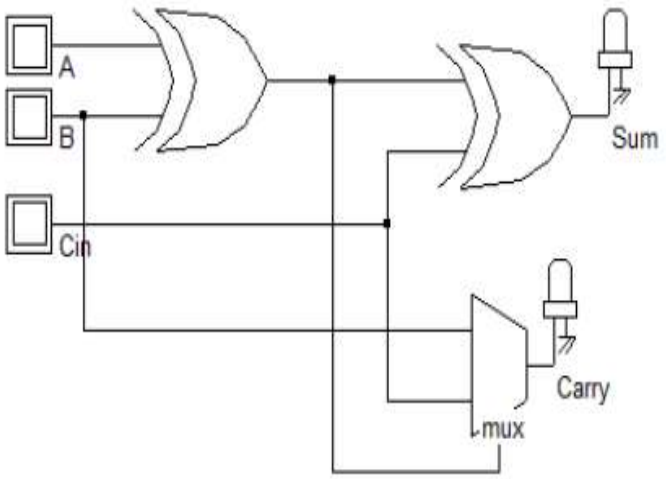

Fig.2: XOR based 1-bit Full Adder

The main difference between the conventional and XOR based adders is that in XOR based adder other than two XOR gates only one 2:1 MUX is used which needs only 6 MOSFETs where as in conventional type adder other than two XOR gates two AND gates and one OR gate is needed which requires at least 18 number of MOSFETs. So, there is at least 12 numbers of MOSFET savings in XOR based 1-bit adders than conventional which in turn has less area and power consumption at the same time there is also a better delay performance.

3.2 Carry Select Adder

The CSA is constructed from two RCAs and a multiplexer. Addition of two n-bit numbers with CSA is nothing but adding two numbers taking input carry first as zero then using another adder taking input carry as one. After calculation of the two results depending on the correct carry-in the correct sum as well as the correct carry-out is selected with the multiplexer connected at last to get the final output. The structure of a 16-bit CSA is shown in Fig. 5.

A 16-bit CSA consists of 16-full adders with the carry signal that ripples from one full adder stage to the next, i.e. from LSB to MSB. The layout and input-output wave shapes of a 4-bit CSA are shown in Fig. 6 and Fig. 7 respectively. Due to clarity of the pictures, layout and input output waves of 4-bit CSA are given here in place of 16-bit adder. Results of 16-bit CSA will be given later. Since XOR based 1-bit adders have been used in the 16-bit CSA

which are the main building blocks so the number of MOSFETs required is much less than conventional CSA.

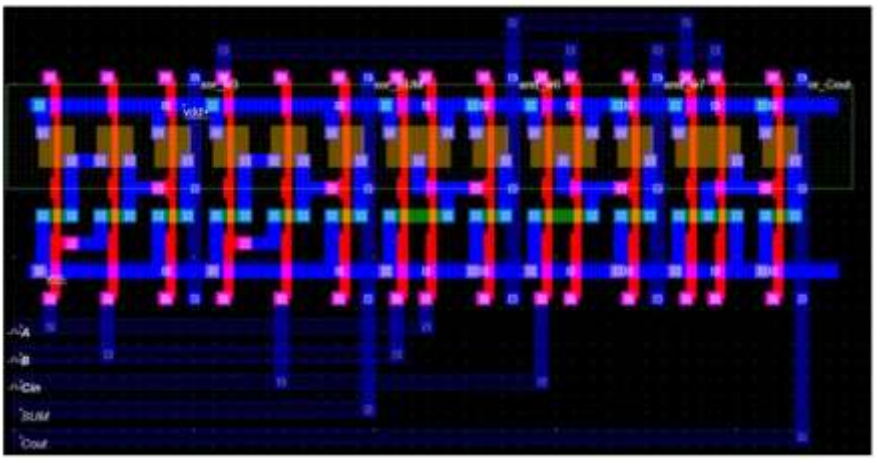

Fig.3: Layout of conventional 1-bit full adder

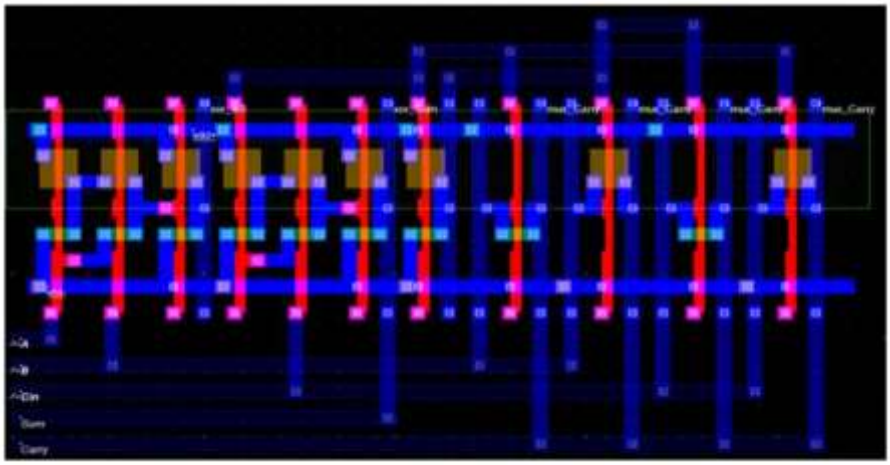

Fig.4: Layout of XOR based 1-bit full adder

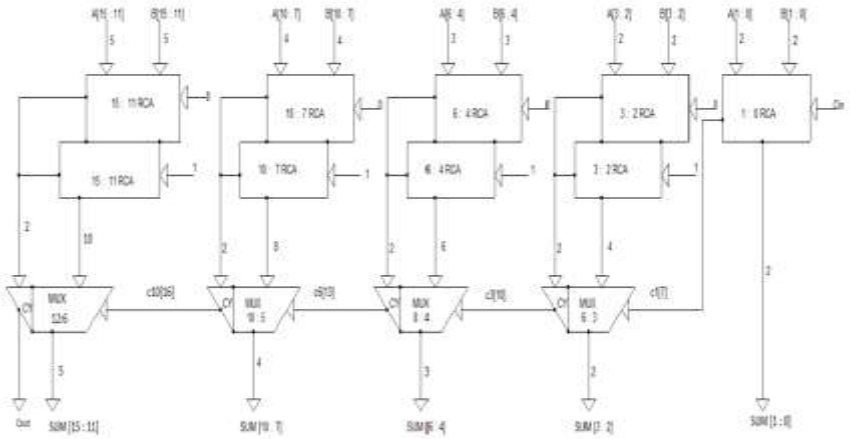

Fig.5: 16-bit carry select adder

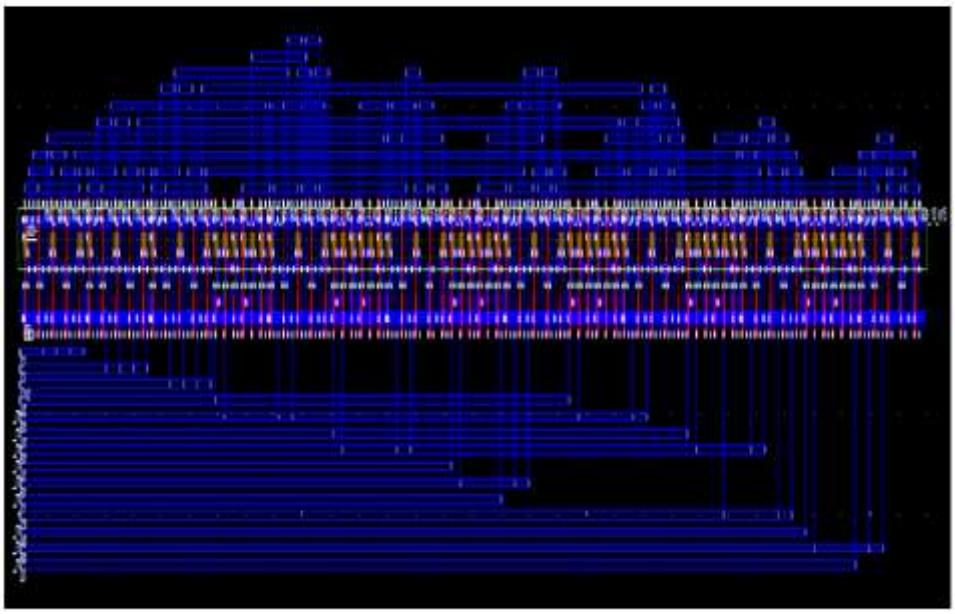

Fig.6: Layout of 4-bit carry select adder

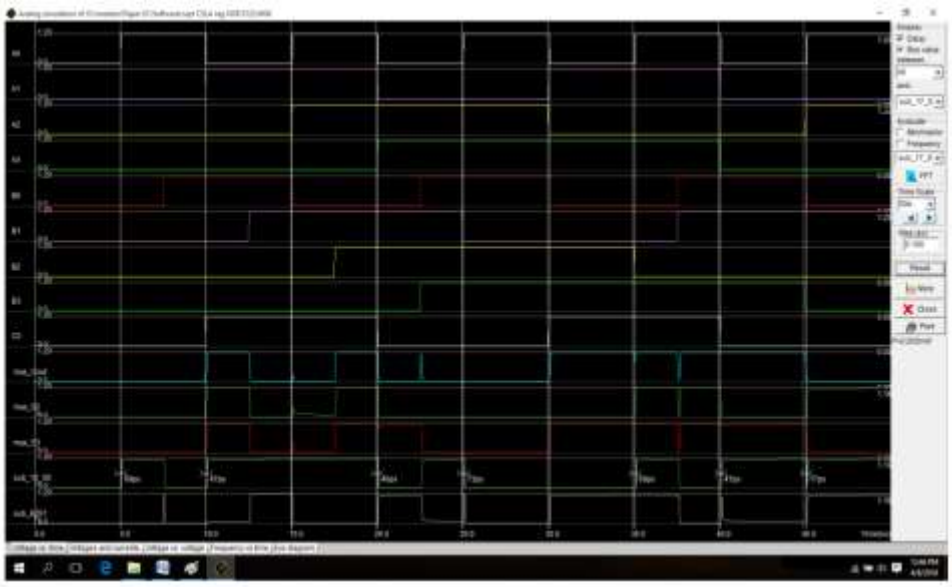

Fig.7: Input-output wave shapes of a 4-bit carry select adder

4. Results and Discussion

The schematic circuit of the CSA has been designed using DSCH 3.1 simulator and synthesized using 90 nm CMOS technology. The layout was constructed from the Verilog file which is generated from the DSCH software. The obtained power, area and delay information of the adder is from Micro wind layout simulation.

Table I shows the simulation results of both conventional and modified CSA (using XOR based adder) in terms of power, area, delay and power delay product (PDP). Every individual

cell in the design adds to the aggregate cell zone and total power is the sum of leakage power, switching power and static power. The XOR-based circuit has the power reduction for 4-bit, 8-bit and 16-bit are 12.5%, 16.67% and 20.04% respectively. Similarly percentage reduction in area are 1.35%, 6.6% and 9.41% respectively. There is also a delay reduction of 0.8%, 1.3%, and 2.01% respectively. In Table II, gate count and Idd values are shown for 4-bit, 8-bit and 16-bit CSA respectively. In Table III, power, delay and area for 8-bit and 16-bit adders are compared with Reference.

TABLE I. COMPARISON OF POWER, AREA AND DELAY BETWEEN CONVENTIONAL CSA AND XOR BASED CSA

Bit size	Adder	Power (mW)	Area (μm^2)	Delay (ns)	PDP (pWSec)
4-Bit	Conventional CSA	0.232	287.00	2.561	0.594
	XOR based CSA	0.203	283.12	2.538	0.515
	Percentage reduction	12.5%	1.35%	0.8%	13.29%
8-Bit	Conventional CSLA	0.300	580.855	2.520	0.756
	XOR based CSA	0.250	542.485	2.487	0.622
	Percentage reduction	16.67%	6.6%	1.3%	17.72%
16-Bit	Conventional CSLA	2.803	1170.14	5.117	14.34
	XOR based CSA	2.241	1060.01	5.014	11.24
	Percentage reduction	20.04%	9.41%	2.01%	21.62%

TABLE II. COMPARISON OF GATE COUNT, IDD MAX AND IDD AVG BETWEEN CONVENTIONAL CSA AND XOR BASED CSA

Bit size	Adder	Gate count			I_{dd} max (mA)	I_{dd} avg (mA)
		nMOS	pMOS	Total		
4-Bit	Conventional CSA	99	99	198	1.679	0.193
	XOR based CSA	63	63	126	1.389	0.169
	Percentage reduction	36.37%	36.37%	36.37%	17.28%	15.54%
8-Bit	Conventional CSA	195	195	390	2.231	0.550
	XOR based CSA	123	123	246	2.132	0.459
	Percentage reduction	36.93%	36.93%	36.93%	4.44%	16.55%
16-Bit	Conventional CSA	386	386	772	6.626	2.336
	XOR based CSA	243	243	486	5.023	2.316
	Percentage reduction	37.04%	37.04%	37.04%	24.19%	0.86%

Table III: Comparison with other work

Bit size	Parameters	Ref. [5]	This work
8-Bit	Power (mW)	13.598	0.250
	Delay(ns)	2.094	2.487
	Area (μm^2)	952.343	542.485
16-Bit	Power (mW)	29.311	2.241
	Delay (ns)	2.450	5.014
	Area (μm^2)	1901.093	1060.01

5. Conclusion

A 16-bit CSA is implemented in this paper using XOR based 1-bit full adder as a building block. The schematic has been designed in DSCH software and synthesized using 90 nm CMOS technology. The layout has been created and simulated in Micro wind software. From the simulation result 20.40% reduction in power consumption, 9.41% reduction in area and

2.01% reduction in delay have been achieved for an XOR-based 16-bit CSA than conventional CSA. Also 37.04% reduction in gate count and 24.19% current reduction were found.

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