DESIGNING A LOW-POWER PHASE-LOCKED LOOP FOR HIGH-FREQUENCY OUTPUTS IN PERVASIVE WIRELESS APPLICATIONS

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Abstract:- A new design of Phase-Locked Loop (PLL) with multiple outputs in low power and high speed has designed with Noise Efficient System. The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm. The input 1Mhz - frequency of this PLL gotten external source is able to generate multiple frequencies provided for the circuits of communication standard in high-speed Integrated Circuits, such as Serial Peripheral Interface (SPI - 128MHz), Two-wire Interface (I^2C-Ultra fast mode 5Mhz), etc. The PLL is designed with a 45nm CMOS technology and verified under parasitic extraction. The results of this design are shown less than 1mW power consumption and the out range of 4Mhz to 128Mhz during 25-50^oC temperature.

Keywords:- Phase Detector (PD), Noise Efficient System (NES), Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO)

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DOI: 10.53555/ecb/2022.11.7.109

Introduction:-

Phase Locked Loops are usually preferred over other methods of maintaining phase lock such as injection locking. Monolithic phase locked loops have been used for clock-&-data recovery in communication system, clock generation & distribution in microprocessor and frequency synthesis in wireless application. Until DSP technology is capable of directly processing and generating the RF signals used to transmit wireless data, traditional RF engineering will remain a fundamental part of wireless communication systems design.

The reference signal is periodic such as square wave which is compare with the output of VCO using a phase detector. The output of phase detector is then applied to the low pass filter and used as a control signal to drive a VCO. The idea is that the VCO will lock onto reference signal thus can be used to tracked a periodic signal as its phase and frequency varies.

Basic PLL is a feedback system composed of three elements PD, LPF and VCO. Design and analysis of a low power phased-locked loop with multiple output(s) is basically implemented by modifying closed loop frequency control system PLL-blocks as shown in following fig 1.

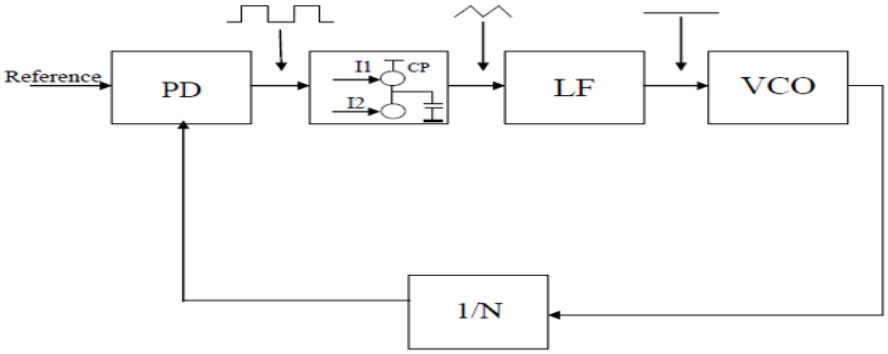

Fig 1: Basic Blocks of PLL

For multiple outputs PLL8x is the basic output of PLL, the 90^{o} phase shifted output can be generated using delay circuits or using logic circuits which is turn offers his speed performance at low power. It would have multiple outputs 1x, 2x, 4x and 8x which can be utilized in multi-phase clocking circuits.

BSIM4 still considers the operating regions described in MOS level 3 (linear for low V_{ds}, saturated for high V_{ds}, subthreshold for $V_{gs}<V_t$), but provides a perfect continuity between these regions as shown. BSIM4 introduces a new region where the impact ionization effect is dominant. The number of parameters specified in the official release of BSIM4 is as high as 300. A significant portion of these parameters is unused in this implementation. Comparison of Voltage & Time Response of Phase Detector is shown in below fig 2.

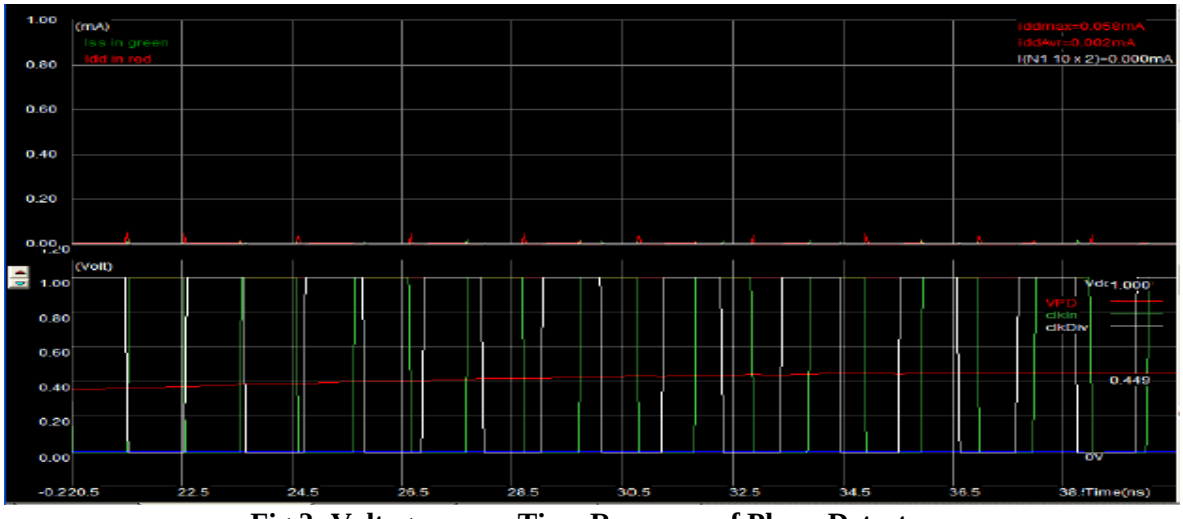

Fig 2: Voltage verses Time Response of Phase Detector

High Performance Voltage Controlled Oscillator (VCO):-

The high performance VCO shown in fig 3, provides very good linearity. The principle of this VCO is a delay cell with linear delay dependence on the control voltage. The delay cell consists of a p-channel MOS in series, controlled by $V_{control}$, and a pull-down n-channel MOS, controlled by V_{plage}. The delay dependence on $V_{control}$ is almost linear for the fall edge. The key point is to design an inverter just after the delay-cell with a very low commutation point Vc.

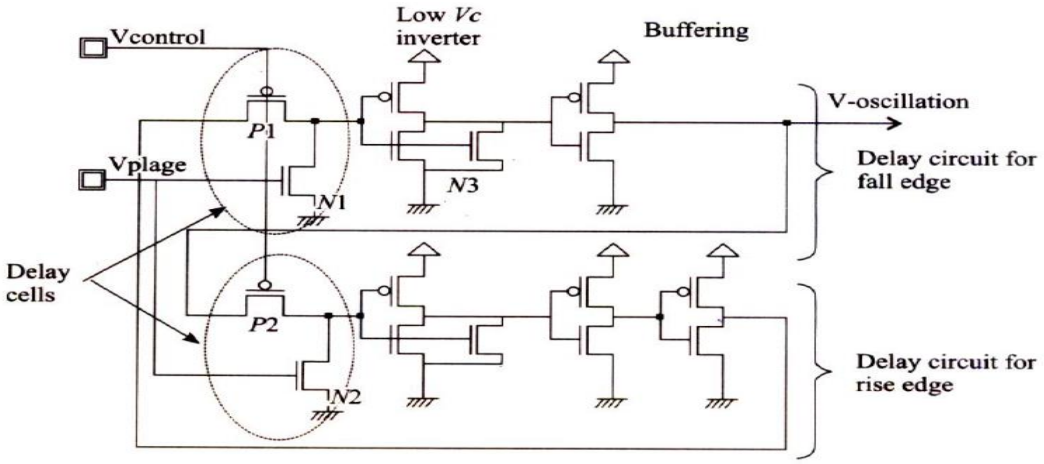

Fig 3: High performance VCO

Phase Locked Loop With High Performance VCO:-

The VCO oscillation is started and the phase detector starts operating erratically. The output of XNOR indicates very interesting that what happens inside the phase detector. We have seen that for the first 10 nanoseconds the phase difference is very important. Then, the VCO outputs starts to converge to the reference clock. In terms of voltage control, Vc tends to oscillate and then converge to a stable state where the PLL is locked and stable. The output is equal to one fourth of the period according to phase detector principles.

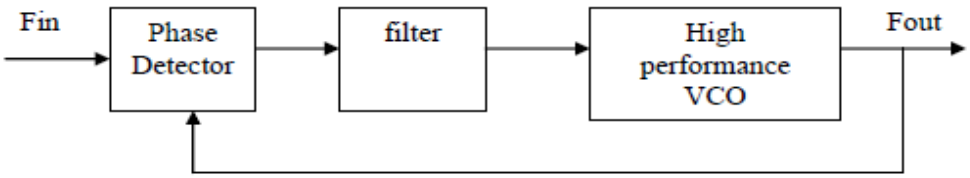

Fig 4: Schematic Diagram of Phase locked loop with High Performance VCO

Low Power PLL with Four Outputs Using 45 nm VLSI Technology:-

Current PLL ICs are highly integrated digital and mixed signal circuits that operate on low supply voltages and consume very low power.

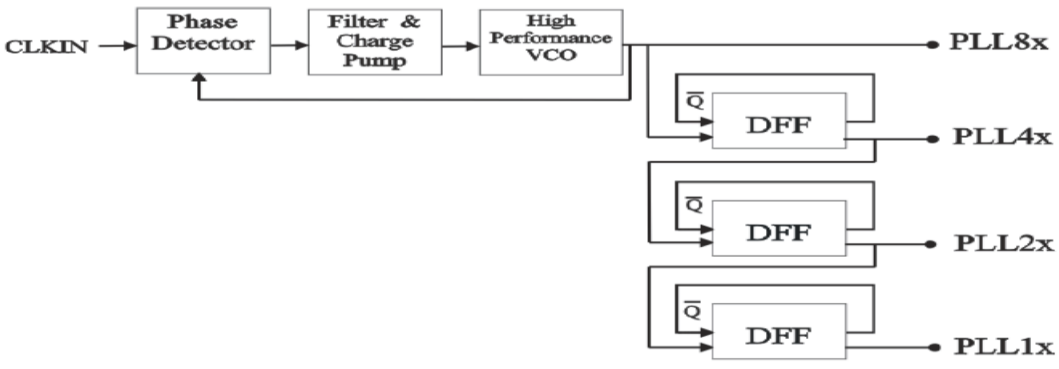

Fig 5: Block Schematic of PLL with four outputs

In above fig 5, it is observed that frequency of clkin is get divided by two at the output div2. For the output section of proposed PLL, the output of VCO Vhigh is represented by PLL8x. The other outputs PLL4x, is obtained by cascading the output of PLL8x as a input to divided by 2 network $D_{register}/D_{flopflop}$. PLL2x is obtained by by giving the output PLL4x as an input to another $D_{register}/D_{flopflop}$. And PLL1x is obtained by giving the output PLL2x as a input to another $D_{register}/D_{flopflop}$ as shown in fig 5.

Conclusion:-

The modeling of CMOS device behaviors are analyzed with the equations including threshold voltage, short channel effect narrow channel effect, electron temperature effect, hot carrier effect and capacitance model. Finally, the BSIM SPICE models BSIM4 are summarized for deep-submicron CMOS transistor. Analysis of Voltage Variation Of V_{DD} On Frequency Of VCO output PLL8x from 0.8V to 1.20V with 3.306GHz.

The parametric analysis of voltage variation of Vdd on frequency of multiple output node shows that frequency for all node are remain stable and minimizes the jitter problems. In this way, very high efficient, low power, highly stable, Layout of chip is designed for phase locked loop with four multiple outputs as PLL8x, PLL4x, and PLL2x & PLL1x.

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