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AXI VIP VERIFICATION USING UVM

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Abstract

AXI is a sub-protocol of ARM Advanced Microcontroller bus architecture (AMBA). This AMBA AXI protocol is focused on high-overall performance and high-frequency design and it consists of capabilities that make it appropriate for high-speed IP interconnect. VIP is a great technique and it's far evolved with the aid of using industry specialists for decreasing the time in the testbench environment. VIP is a built-in structure for verification of on-chip transactions and it's a far gift to the internal of SoC. In this paper, the testbench is written and verified for the Write and Read Transactions between master and slave and also for other test cases like out-of-order transactions, associative arrays, same read write addresses, etc.

Keywords: AMBA, VIP, UVM, AXI, MASTER, SLAVE.

1.INTRODUCTION

The fast growth in the CMOS era and Computer Aided Design results in the utilization of a massive range of IP (Intellectual Property Cores) inside the complicated virtual designs. With the assistance of that IP cores integration, Nowadays the SOC (System on Chip) layout turns into extra famous and intensively used for plenty of applications. Also, all of the SOC layouts make use of bus protocols for making information communique and synchronization. Hence, the reusability of big quantity of IP cores within the complicated layout makes the useful verification manner so crucial (i.e., because it includes 70% percentage of the time span compared to the 30% of the time span for layout technique). In order to triumph over this issue and big time span the verification engineers proposed a method for verifying the capability of the chip the use of a built-in verification surroundings known as Verification IP (VIP).

The coverage model will identify the bugs and errors in the code by comparing the Master

transmitted data to the slave received data. Then it validates the functional behavior of thedesign for the test cases.

2.PROBLEM STATEMENT

In AXI protocol there is a limitation because a single master communicates with a single slave only at a given instant. The proposed design will give better parallelism between multiple masters and multiple slaves.

In protocol AXI there is a limitation to using arbitration technique in multiple masters and multiple slave situations, which makes the overall system complex

but the proposed design will use AXI VIP protocol which supports different IDs and instead of arbiter use channel handshaking, it supports burst transfer, working for incr and fixed, working for wrap, queue for fixed, associative for burst and incr, outstanding transaction.

3. OBJECTIVES

Themain objective of this paper is:

- The main objective of the project is to interface the master with the slave with the help of the AXI bus system.
- Here master can write the data in the slave memory or it can read the data from the slave memory directly using AXI bus protocols.
- Data can be transferred in the form of a burst which is nothing but a bunch of data in the form of bytes.
- Master sends only the initial address location of the memory to be written or to read from. The rest of the data is transferred according to the initial address.
- AXI is used in data for better accuracy and efficiency.
- The verification method is developed in the System Verilog, simulated on EDAplayground.

3.1.RELATEDWORKS

PAPER1: Testing of AMBA AXI protocol.

Thispaperwas published intheyear 2022byTanupriya A G, Kiran V.

This paper gives an overview of AMBA protocol and designed the AXI Master and slave using Verilog HDL and System Verilog was used to verify the DUT. The basic transactions of the Master and Slave were verified. And the System Verilog Language provides simplicity, better flexibility, efficiency and system reusability.

PAPER 2: Design and SV-based verification of AMBA AXI protocol for SoC integration.

This paper was published in the year 2019 by Intel Rashmi Samanth, and Subramanya G Nayak.

This paper focused on the general design implementation of AXI master-slave transaction using SRAM as a slave using Verilog HDL, Design challenges are discussed, SV based verification methodology is implemented to check the performance of the design.

3.2 SPECIFICATIONS

VIP Architecture block diagram is on the upcoming page and according to that block diagram, we have written the code in System Verilog in the EDA playground. For every single block the code is separately written and then the functions are interlinked and called in the top module of the code. When the code is simulated in the EDA playground, we can obtain the waveforms which show the Master-Slave Transactions and verify the test cases.

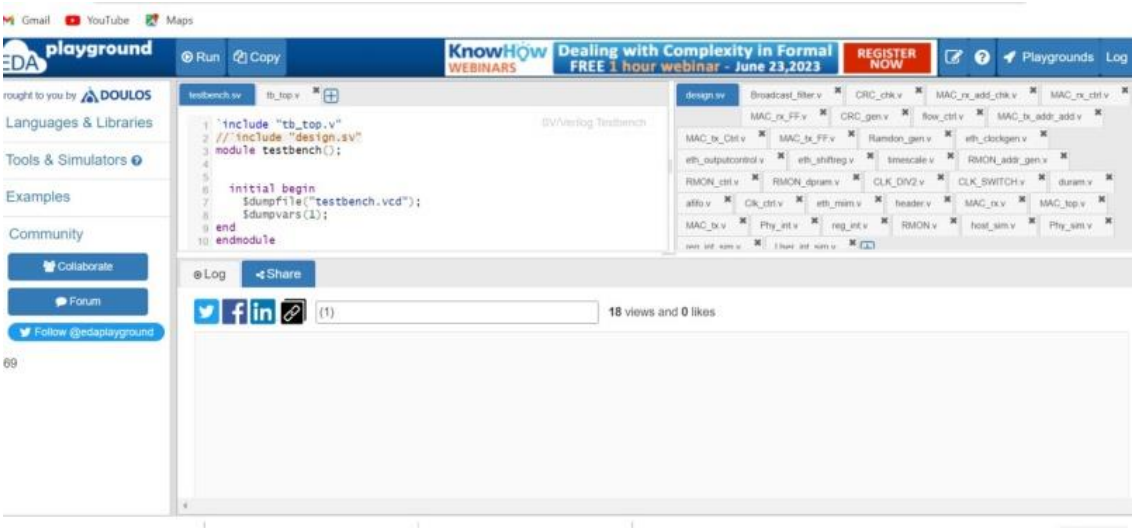

Fig.1. EDA Playground.

4.METHODOLOGY

Different features of the AXI protocol are verified by developing the VIP. Below is the configurable UVM TB architecture used to verify the protocol.

The configurable parameters include the number of master agents, number of slave agents, active & passive agents, a virtual interface, etc.,

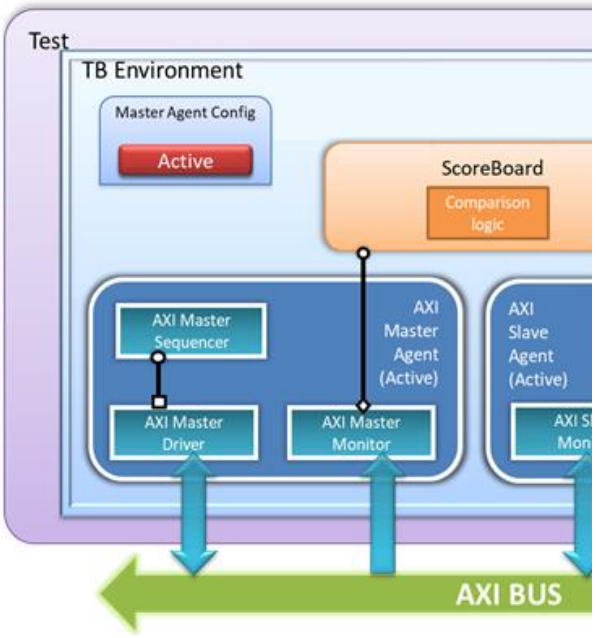

Fig.2.AXI VIP.

AXI VIP consists of the following:

- **AXI Test**: The test class encloses the environment and set the configuration object in the config database. In the run phase, the test starts the stimulus generation by starting the sequence.
- **AXI Environment**: It encloses different uvm components like agents, scoreboard, virtual sequencer, etc required for TB based on the configuration parameters and also connects the agent monitors with the scoreboard using the TLM interface.
- **AXI Master & Slave agents**: It enclosesthe monitor, driver, and sequencer based on the is active value in the configuration database and connects the driver and sequencer using the TLM interface.
- **Sequence Item**: Data item based on the DUT protocol.
- **Sequence**: Generates sequence items.
- **Sequencer**:Routes the sequence items from sequence to driver
- **Driver:**Drives the transaction level signals on to interface as per the DUT protocol.
- **Monitor**: Collects the interface signals and converts them into transactions and broadcasts the

transactions to the scoreboard, coverage models, etc.,

- **Scoreboard:** Compares the reference data with DUT and implements the coverage models.
- **Configuration Object:** A container object, used to pass information from the test to the lower-level components which affect what lower-level components do and how they are built and connected.

5.FEATURES

- Supports all protocol data widths and addresses widths, transfer types, and responses.
- Full AXI Protocol Checker support.
- Integrated ARM Licensed Protocol Assertions.
- Transaction level protocol checking (burst type, length, size, lock type, cache type).
- Behavioral System Verilog Syntax.
- System Verilog class-based API.
- Configurable simulation messaging.
- System Verilog example designs and test benches delivered in IP Integrator.
- Supported Simulators: Aldec Riviera-PRO, Cadence Incisive Enterprise Simulator, Vivado Simulator, Mentor Graphics Questa Prime, and Synopsys VCS.

6. RESULT ANALYSIS

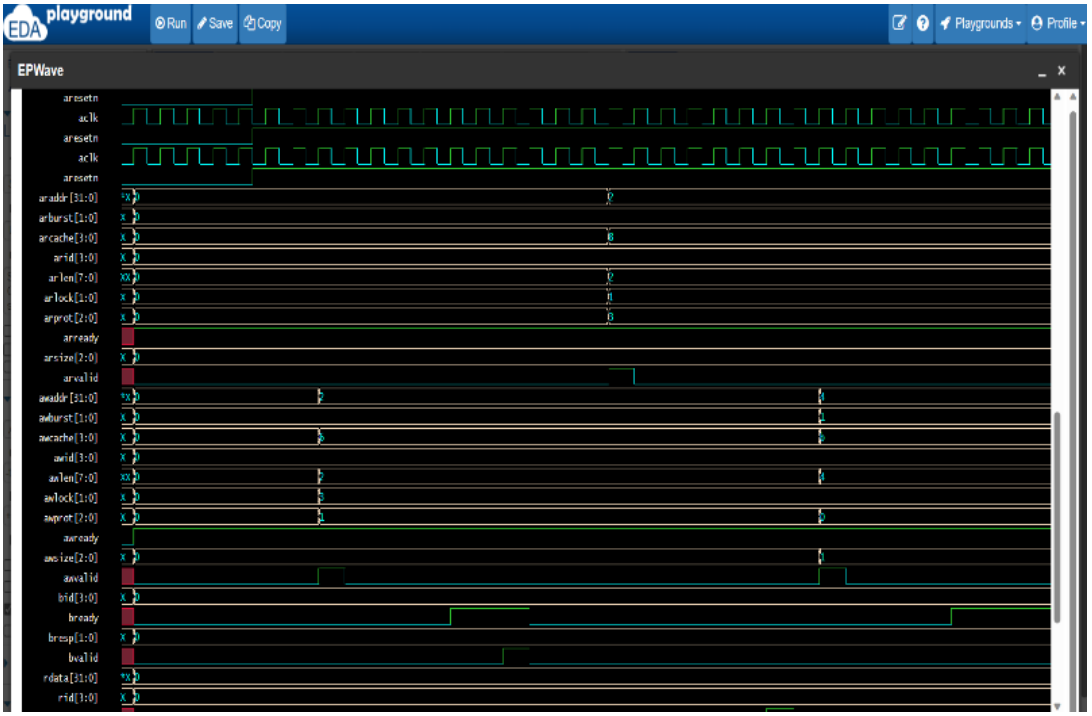

Fig.2.Graph representing Output wave forms

7. CONCLUSION

AXI is a mainstream protocol used in SoCs for High speed and Low Latency. The advancement in the technology leads to better and better implementation of test benches to verify operations, by using VIP with UVM we can overcome these challenges and provide reusable IP for SoCs design thus reducing time to market. Transactions between Master and Slave are verified for different scenarios like, read and write operations, out-of-order transactions, and same address read-write, wrapping, INCR, etc. These verified IPs can be used for future purposes as it is or can alter as per the requirement or according to the need.

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