LOW DROP-OUT REGULATOR WITH HIGH PSRR USING POLE SPLITTING SCHEME

Sushroot[1], Dr. Syed Hasan Saeed[2]

Article History: Received: 12.12.2022 **Revised:** 29.01.2023 **Accepted:** 15.03.2023

Abstract

Presently analysis of poles and zeros in a circuit is important for choosing the topology for defining the specifications, understanding the frequency response and enhancement of the circuit stability by applying compensation. such type of analysis are also included in low-dropout (LDO) voltage in control loop for small analysis of signal by placement of poles by regulating the load current at output terminal. This paper is focusing the objective for providing a step-by-step process for analysis of poles and zeros in LDO's. Process of frequency compensation techniques are involved to get high power supply rejection ratio (PSRR) with stable frequency response .

Keywords: Low-dropout (LDO) voltage regulator, pole zero compensation, power supply rejection ratio (PSRR), Frequency compensation.

[1]Integral University, Dept. Electronics & Communication Engineering, Lucknow, India
[2]Integral University, Dept. Electronics & Communication Engineering, Lucknow, India

Email: sushrutpankaj@gmail.com[1], ssaeed@iul.ac.in[2]

DOI: 10.31838/ecb/2023.12.s3.269

1. Introduction

A desire to implement mixed signal systems on a single chip is being sparked by the increasing density of digital CMOS processes and recent advancements in digital signal processing. For a single chip implementation, an accurate current reference is needed to perform conversions between the digital and analogue domains.

Regulating an output voltage powered by a higher voltage input with the help of LOW DROP-OUT DC-DC REGULATORs is a straightforward and cost-effective procedure. They are simple to use and design with. The parameters of a LOW DROP-OUT DC-DC REGULATOR datasheet are typically very clear and simple to comprehend for the majority of applications. However, in some applications, the designer must look more closely at the datasheet to see if the LOW DROP-OUT DC-DC REGULATOR is appropriate for the particular circuit conditions. Unfortunately, datasheets do not cover all operating conditions and parameters [1].

Low Drop-Out Dc-Dc Regulator Regulators

The purpose of voltage regulators is to provide a stable voltage for the power supply that is unaffected by changes in the input voltage, temperature, time, or load impedance. The ability of low-dropout regulators to maintain regulation despite minute variations in supply voltage and load voltage is what sets them apart.

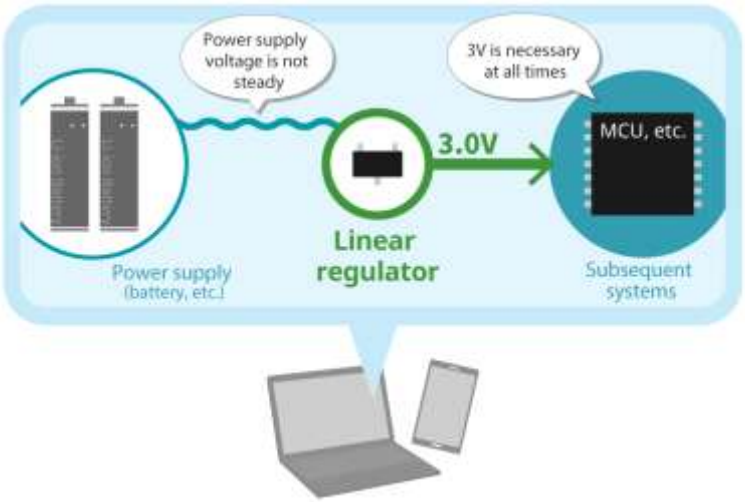


Figure 1: Graphic representation of the roles of a linear regulator in electronic devices

When a lithium-ion battery declines from 4.2 V when fully charged to 2.7 V when almost depleted, a LOW DROP-OUT DC-DC REGULATOR may keep a steady 2.5 V at the load as an illustration. A straightforward explanation of the fundamental functions of a typical LOW DROP-OUT DC-DC REGULATOR can be found in Figure 1.

As a result, designers are considering LOW DROP-OUT DC-DC REGULATORs to keep the battery charge constant while maintaining the necessary system voltage. This is brought on by the rise in the use of portable applications. However, LOW DROP-OUT DC-DC REGULATORs might be useful for more than just portable systems. A candidate for LOW DROP-OUT DC-DC REGULATORs is any piece of equipment that requires a constant voltage while minimizing the upstream supply (or working with large upstream supply fluctuations). Digital and RF-loaded circuitry are typical examples.

Related Work:

Lee Yong-Jin and others proposed digital low drop-out (LDO) regulators with a load capacity of more than 200 mA and a quick transient response in a coarse-fine dual-loop design. in 2016 [23]. The proposed approach makes use of the coarse loop and the fine loop to co-regulate the output voltage. The coarse loop uses a quick current-mirror flash analog to digital converter and produces a lot of output current to improve transient performance. The fine loop, on the other hand, contributes to the reduction of voltage ripples, produces little output current, and improves regulation precision. In addition, a computerized regulator is utilized to avoid conflict between the two circles. The suggested digital LDO is made using the Samsung CMOS process, which has a node size of 28 nm and a chip area of 0.021 mm2. When the input and output voltages are 1.1 V and 0.9 V, respectively, it can handle a maximum load of 200 mA. A low-dropout (LDO) voltage regulator is the primary component of the majority of portable electronic applications because it serves as a power management system. S.A.Z. Murad and others discovered that the actual output voltage drop for a

load step of 180 mA was approximately 120 mV. describe an LDO regulator based on Cadence software for a power management integrated circuit that makes use of 0.18-m CMOS technology. al., (2019) [24]. The error amplifier that has been suggested for the LDO consists of seven transistors that act as the current mirror. The PMOS transistor serves as a pass element transistor while voltage variation is managed. The resistors function as a feedback network circuit while the capacitor reduces variation in the output voltage. Jorge Pérez-Bailón et al. propose a 27 x 34 m layout, 1.0 mV/V line regulation, 0.41 mV/A load regulation, constant output voltage of 2.41 V for supply voltage ranges of 2.55 V to 3.55 V, 140 mV dropout voltage, and 1.48 mW power consumption. presented an affordable low dropout (LDO) regulator that is fully integrated into a standard 180 nm CMOS technology and does not use capacitors. in 2021. Over a temperature range of -40 to 120 °C, this regulator regulates the output voltage of a 3.3 V to 1.3 V battery at 1.2 V. In order to meet the requirements of battery-operated system-on-chip (SoC) devices, which include maintaining an ultralow power consumption of 8.6 A and a minimum area consumption of 0.109 mm2, a high-gain dynamically biased folded-based error amplifier topology that is optimized for low-voltage operation is utilized.

A novel dual loop topology-based capacitor-free low dropout (LDO) linear regulator was presented in 2021, according to Yoni Yosef-Hay and colleagues [26]. Hearing aid issues like brief voltage spikes during rapid changes in load-current and rapid transient performance are addressed by the regulator through feedback loops. The proposed layout, which operates with a capacitive load of 0-100 pF and does not require an off-chip discrete capacitor connected at the output, was implemented using 0.18 m CMOS technology. The suggested regulator is suitable for system-on-chip integration due to its low component count. At a voltage of 64 mV, a 250-500 A current step load has a settling time of 3 s and an edge time (rise and fall time) of 1 ns when CL is zero. From a range of 1.0 V to 1.4 V, it adjusts the output voltage to 0.9 V. The power supply rejection ratio, or PSRR, is 63 dB at 1 kHz.

2. Methodology

A linear voltage regulator that reduces a DC voltage (from a battery, a DC-DC converter, etc.) is known as an LDO. from its source to its destination. An LDO's input voltage might not be the best DC voltage. For instance, if the LDO's input voltage comes from a DC-DC converter, it might have ripple that hurts the electronic devices it powers. Voltage ripple can be reduced by the LDO. Nowadays, the LDO's PSRR, or ability to reduce power supply ripple, is regarded as crucial. In the past, the low-frequency region required a high PSRR, but nowadays, both the low-frequency and high-frequency regions frequently require very high PSRRs. The PSRR's fundamentals, including its frequency dependence, are provided in the subsequent sections.

The equation that follows describes an LDO's PSRR, or its capacity to reduce ripple on the input voltage (VIN). The waveform of the output voltage supplied to its load and a typical LDO with a PMOS pass device are depicted in the figure below.

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}}\ (dB)$$

V_{INRPL}: Ripple on the input voltage (V_{IN}) of the LDO
V_{OUTRPL}: Ripple on the input voltage (V_{IN}) of the LDO

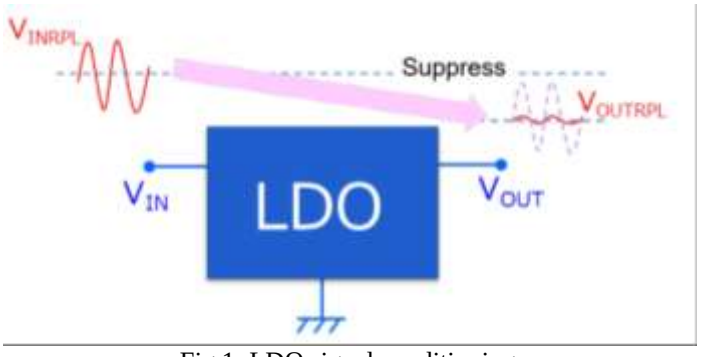


Fig.1: LDO signal conditioning

A. Frequency dependence of the LDO's PSRR:

The PMOS pass device's gate voltage changes simultaneously with VIN while maintaining a constant voltage difference if the ripple on the gate voltage is the same as the ripple on VIN (VINRPL). Due to the VIN ripple, the PMOS pass device does not transmit any current to the output in this instance. This is correct because theoretically, the PMOS pass device's gate voltage and input voltage (VIN) have the same ripple. The

ratio of an LDO's (low impedance with negative feedback) output impedance (ZOUT) to the PMOS pass device's output resistance (rDS) is used to divide the VIN ripple voltage in this instance. This voltage division ratio thus determines PSRR.

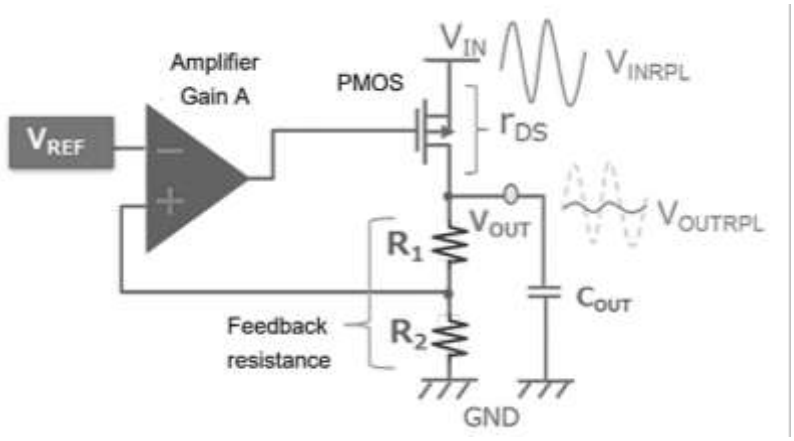
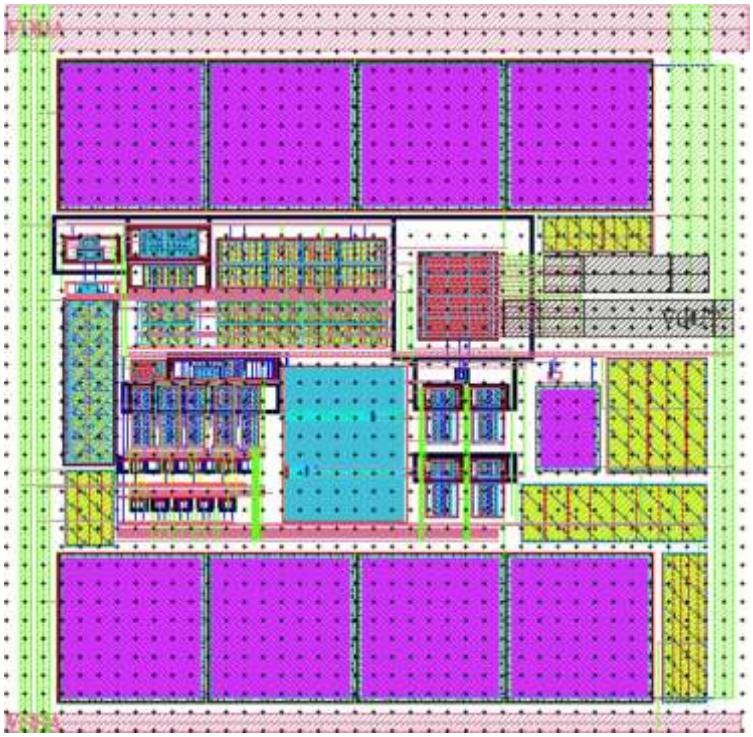


Fig. 2: PSRR depiction in LDO design

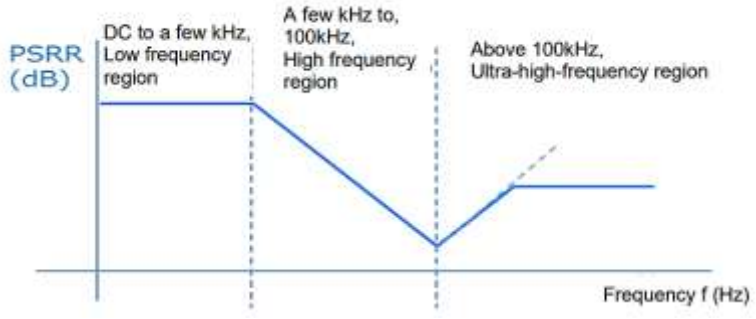
$$PSRR\ definition: PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{OUT} + r_{DS}}{Z_{OUT}}\ (dB)$$

Negative feedback has resulted in the LDO's low output impedance (ZOUT) (ZOFB, which will be discussed further). To achieve low output impedance, the internal amplifier's gain is an important factor. PSRR is also influenced by frequency because of the amplifier gain's dependence on frequency.

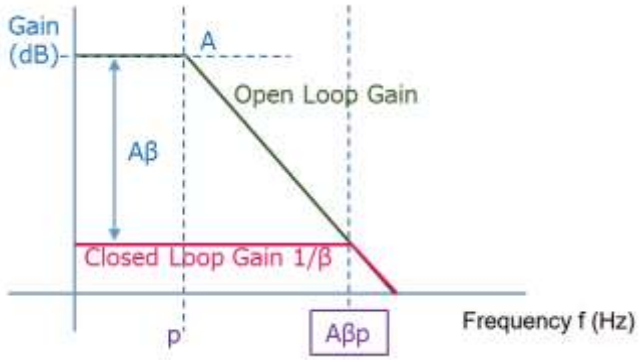


B. Details of the frequency dependence of LDOs:

The LDO's PSRR is influenced by frequency. In most cases, the LDO has a high PSRR in the low frequency range and a lower PSRR in the high frequency range. An LDO's PSRR can be divided into three frequency regions: 1) The low-frequency region between DC and a few kilohertz (the "low-frequency region"), 2) The high-frequency region between a few kilohertz and 100 kHz (the "high-frequency region"), and 3) The ultra-high-frequency region above 100 kHz (the "ultra-high-frequency region").

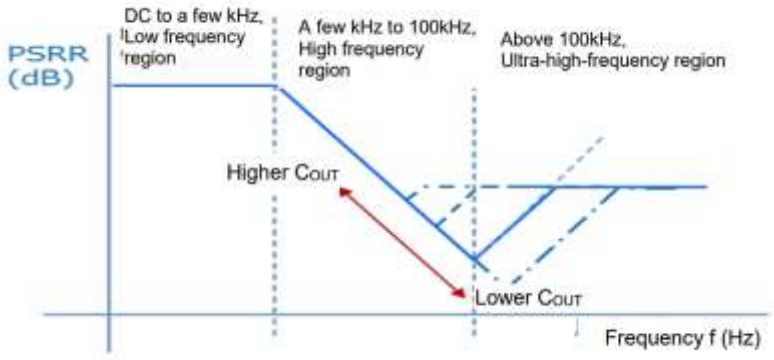


At frequencies close to the boundary between the low-frequency and high-frequency regions, the PSRR equation can essentially be utilized. The output capacitor (COUT) can be thought to have no effect on PSRR at these frequencies. However, in contrast to the low-frequency region, the internal amplifier's gain (A) is frequency-dependent.



According to the negative feedback hypothesis, the closed-loop transfer function's cut-off frequency is A times that of the open-loop transfer function, or Ap. It is believed that Ap is near the ultra-high-frequency region's boundary.

Because its impedance is solely determined by capacitance and varies with frequency, the output capacitor (COUT) functions as a pure capacitor at low frequencies. However, when frequency reaches a certain threshold, the equivalent series resistance (RESR) takes precedence and the impedance of COUT decreases to almost zero. The COUT impedance dominates at frequencies close to the ultra-high-frequency and high-frequency boundaries. First, let's look at how PSRR is affected by COUT's capacitance at these frequencies.



In the high-frequency region, PSRR decreases. Because it has a lower capacitive impedance (i.e., a larger COUT), a larger capacitor (COUT) causes PSRR to rise once more at a frequency that is closer to half that of the input signal. As a result, a substantial output capacitor aids in maintaining a high PSRR at high frequencies. On the other hand, PSRR continues to decrease up to a relatively high frequency when the output capacitor (COUT) is small. The equivalent series resistance (RESR) is assumed to be constant.

3. Results and Discussion

PSRR is higher with a 22-µF output capacitor (COUT) than with a 2.2-µF capacitor. PSRR begins to rise at a low frequency of around 100 kHz when using a 22-µF output capacitor, as shown below.

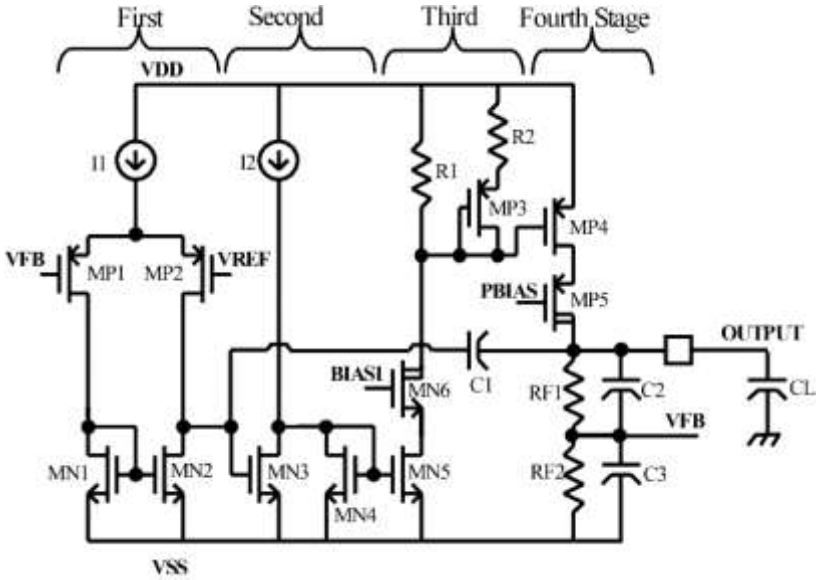


Fig. Conceptual architecture of LDO design

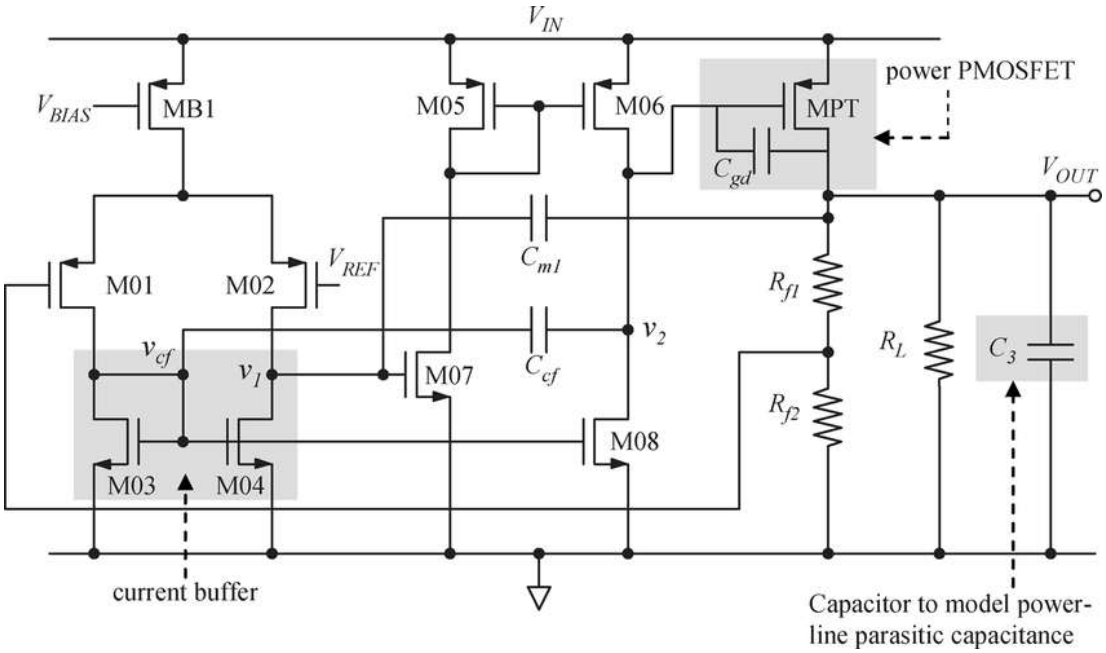
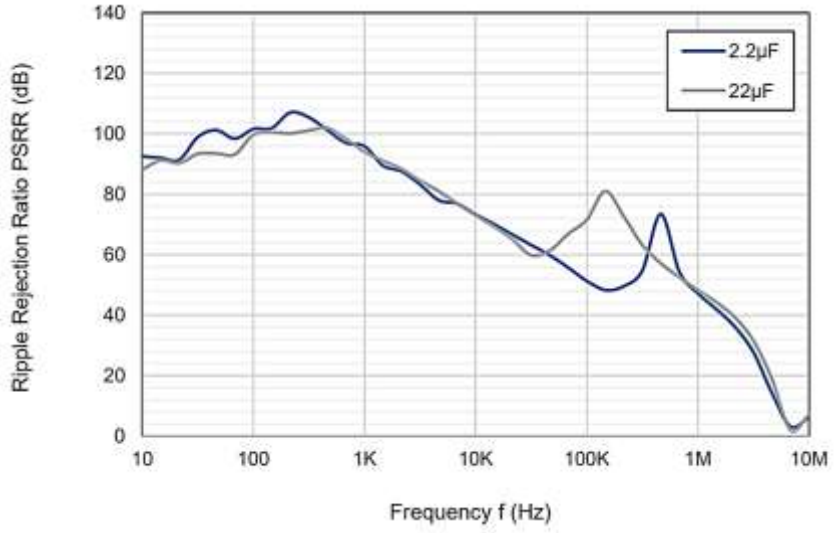
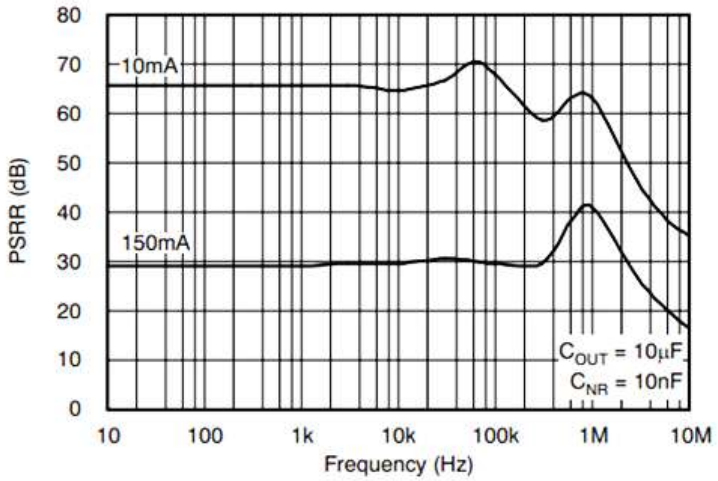


Fig. Schematic of Proposed LDO in 65nm CMOS process

Test conditions: VIN = 1.35 V, VBIAS = 3.3 V, CIN = open, COUT = 2.2/22 µF, IOUT = 10 mA



(a)



(b)

Fig (a) PSRR vs freq. for different CL (b)for different load current

Figure 2 shows the output voltage and input voltage of the 3.0-V ADM7172 LDO. The device is inoperable below 2.3 V, and the dropout region ranges from approximately 3.172 V to 2.3 V. At 2 A, the dropout voltage is typically 172 mV, making RDSON approximately 86 m. At lower load currents, the dropout voltage decreases proportionally: A low dropout voltage of 86 mV at 1 A maximizes the efficiency of the regulator..

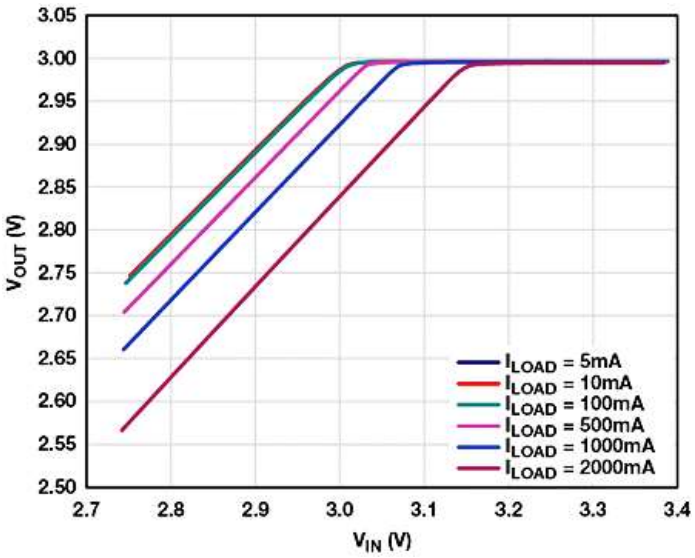


Fig. Dropout region of the proposed LDO Design

Even at high frequency, a high PSRR is now required. When choosing LDOs, PSRR is one of the most important factors. Utilizing an output capacitor (COUT) with maximum capacitance and low equivalent series resistance (RESR) is efficient for increasing the PSRR. However, when selecting LDOs, inrush current and oscillation should also be taken into account. The internal amplifier has a high DC gain and a good frequency response, so these LDOs are more susceptible to oscillation and draw more supply current. However, LDOs with a high PSRR are preferred.

The ground current as well as the voltages at the input and output of an LDO determine its efficiency:

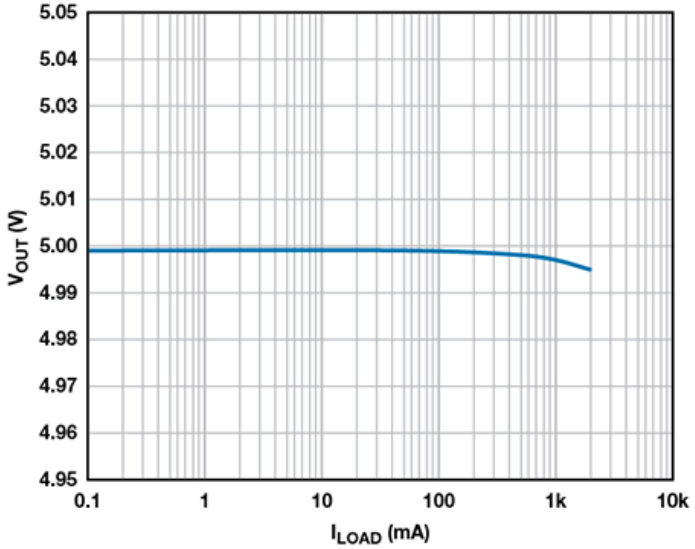
Efficiency = $I_{OUT}/(I_{OUT} + I_{GND}) \times V_{OUT}/V_{IN} \times 100\%$

The headroom voltage and ground current must be kept to a minimum for maximum effectiveness. Additionally, minimizing the voltage difference between the input and output is essential. The voltage contrast between the info and result is a key perspective in deciding effectiveness, no matter what the heap. When powered by 5 V, a 3.3-V LDO's efficiency will never exceed 66%; however, when the input voltage is decreased to 3.6 V, the efficiency will reach 91.7%. An LDO's power dissipation is $(V_{IN} - V_{OUT}) I_{OUT}$.

DC Load Regulation

An LDO's capacity to maintain the desired output voltage under a variety of load conditions can be evaluated using load regulation. Figure 6 shows how load guideline is depicted as

Load regulation = $\Delta V_{OUT}/\Delta I_{OUT}$



Output voltage vs. load current for the proposed LDO design

4. Conclusion

The LDO circuits are getting high popularity in portable devices like laptops and mobile and automotives industries for maintaining low quiescent current and voltage application to keep the long battery life. This paper is based on the enhancement of PSRR in LDOs to supply optimum power at without large variation in the input supply voltage with high gain in desired frequency band. The dominant pole due to output load highly degrades the quality factor of LDO. To suppress its effect a pole splitting concept is added on to reduce the dominant pole effect. The resultant frequency response is observed to be tend tower narrow at peak values for desired frequency band.

Acknowledgement:
All authors would like to thank Integral University, Lucknow for providing the manuscript number **IU/R&D/2023-MCN0001931** for the present research work

5. References

G. Alfonso and R. Mora, "Analog IC design with low-dropout regulators," McGraw Hill New York, 2009.

H. Armani and H. Cordonnier, "Power and battery management ICs for low-cost portable Electronics", Annales Telecommunications Juilet/Aout, vol.59, pp. 974-983, Jul. 2004.

C. Simpson, "A User's Guide to Compensating Low-Dropout Regulators", National Semiconductor, 1997.

G. A. R.-Mora and P. E. Allen, "Optimized Frequency-Shaping Circuit Topologies for LDO's," in IEEE Transactions on Circuits and Systems—ii: Analog and Digital Signal Processing, vol. 45, pp.703-707, June 1998.

Gabriel A. Rincon-Mora and Phillip E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator," IEEE Journal of Solid-State Circuits, Vol. 33, pp. 36-43, Jan. 1998.

G. A. Rincon-Mora, "Current efficient, low voltage, low drop-out regulators," Ph.D. dissertation, Elect. Comp. Eng. Dept., Georgia Inst. of Technology, Atlanta, 1996.

Texas Instruments, "Fundamental Theory of PMOS Low Drop-out Voltage Regulators," Application Report, Apr. 1997.

Jerome Patoux, "Low Drop-out Regulators," Analog Dialogue, May 2007.

P. Phillip, E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford University Press, pp. 246-301, 2002.

K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," IEEE Journal of Solid State Circuits, vol. 38, pp. 1691–1702, Oct. 2003.

X. Lai, J. Guo, Z. Sun and J. Xie, "A 3-A CMOS low-dropout regulator with adaptive Miller compensation," Analog Integrated Circuit Sig. Process, vol. 49, pp. 5-10, Oct. 2006.

W. Oh and B. Bakkaloglu, "A CMOS Low-Dropout Regulator with Current-Mode Feedback Buffer Amplifier," IEEE Transactions on Circuits and Systems—II: Express Briefs, vol. 54, pp. 922-926, Oct. 2007.

M. Al-Shyoukh, H. Lee and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation," IEEE Journal of Solid-State Circuits, vol. 42, pp. 1732-1742, Aug. 2007.

T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," IEEE Transactions on Circuits and Systems—I: Regular Papers, vol. 55, pp. 1392-1401, June 2008.

A. Saberkari, E. Alarco and S. B. Shokouhi, "Fast transient current-steering CMOS LDO regulator based on current feedback amplifier," Integration, the VLSI Journal, vol. 46, pp. 165-171, Mar. 2013.

C. K. Chava and J. Silva-Martinez, "A Frequency Compensation Scheme for LDO Voltage Regulators," IEEE Transactions on Circuits and Systems—I: Regular Papers, vol. 51, pp. 1041-1050, June 2004.

P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan and S. Borkar, "Area-Efficient Linear Regulator with Ultra-Fast Load Regulation," IEEE Journal of Solid-State Circuits, vol. 40, pp. 933-940, Apr. 2005.

Z. Yan, L. Shen, Y. Zhao and S. Yue, "A Low-Voltage CMOS Low-Dropout Regulator with Novel Capacitor-Multiplier Frequency Compensation," IEEE International symposium on Circuits and Systems, pp. 2685-2688, May 2008.

Y. Shiyang, Z. Xuecheng, Z. Zhige and C. Xiaofei, "A Loop-Improved Capacitor-less Low-dropout Regulator for SoC Power Management Application," IEEE Asia-pacific Conference on Power and Energy Engineering, vol. 10, pp. 1-4, Mar. 2009.

J. Hu, W. Liu and M. Ismail, "Sleep-mode ready, area efficient capacitor-free low-drop-out regulator with input current-differencing," Analog Integrated Circuit Sig. Process, vol. 63, pp.107-112, Jan. 2010.

Z. Kamal, Q. Hassan and Z. Mouhcine, "Full On-Chip Capacitance PMOS Low Dropout Voltage Regulator," IEEE International Conference on Multimedia Computing and

systems in Morocco, vol. 54, pp. 1-4, Apr. 2011.

D. Camacho, P. Gui and P. Moreira, "Fully on-chip switched capacitor NMOS low Drop-out voltage Regulator," Analog Integrated Circuit Sig. Process, vol.65, pp.141–149, Jan.2010.

Yong-Jin Lee et. al., "A 200-mA Digital Low Drop-Out Regulator With Coarse-Fine Dual Loop in Mobile Application Processor", IEEE Journal Of Solid-State Circuits 2016.

S.A.Z Murad et. al., "Design of CMOS Low-Dropout Voltage Regulator for Power Management Integrated Circuit in 0.18-µm Technology", The 2nd International Conference on Applied Photonics and Electronics 2019.

Jorge Pérez-Bailón et. al., "A Fully-Integrated 180 nm CMOS 1.2 V Low-Dropout Regulator for Low-Power Portable Applications", Electronics 2021,

Yoni Yosef-Hay et. al., "Capacitor-Free, Low Drop-Out Linear Regulator in a 180 nm CMOS for Hearing Aids", In Proceedings of 2021 IEEE NorCAS Conference IEEE. https://doi.org/10.1109/NORCHIP.2016.7792888