ISSN 2063-5346

A DESIGN OF A RECONFIGURABLE NETWORK-ON-CHIP FOR NEXT GENERATION FPGAS USING DYNAMIC PARTIAL RECONFIGURATION

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Article History: Received: 01.02.2023 **Revised:** 07.03.2023 **Accepted:** 10.04.2023

Abstract

Nowadays the emergence for high speed digital system in VLSI industry and the integration of more number of processing blocks – regulating the data flow and switching activity is becoming most challenging task than ever and significantly affect both circuit life and reliability. The System-on-Chip (SoC) application comes with the integration several Intellectual Property (IP) cores to meet the desired functionality. To reduce the number of interconnection and associated power consumption in system on chip (SoC) application network on-chip plays vital role to regulate the traffic among different IP components. In this paer Dynamic Partial Reconfiguration (DPR) is propsoed in NOC router design to maximize the data rate and regulate the traffic rate inside the digital system. Finally to reduce the switching activity the memory components associated to router design the FIFO memory blocks are replaced with valid and request based hand shake protocol is used inside the Network-on-Chip (NoC). It also includes FSM based high level parameterization to select the most suitable NoC configuration size to reduce the computational complexity overhead and leads improved system reconfigurability to maximize the system performance. In addition to this Reconfigurability during NOC routing highly flexible NoCs and enables full customization for dynamic reconfigurable applications. An increasingly popular option for multi-IP systems-on-chip is networking over chip (NoC)-based communication. Many improvements have been made to the NoC's adoption of FPGA-based, dynamically reconfigurable IPs. One method to lower the power usage of the NoC's idle components is to use a run-time scalable NoC that uses dynamic partial reconfiguration (DPR). Nevertheless, the issue of specialised HDL NoC creation tools that divide the NoC rows and columns into distinct components is still unresolved. In this research, we present an approach to describe and build runtime scalable NoC components for Xilinx FPGAs based on UML, MARTÉ, and IPXACT. In order to model the NoC, it is divided into static sub-NoCs and a component consisting of a sequence of run-time scalable rows and columns.

INDEX TERMS **FSM, NOC configuration Network on chip (NoC), IP, FIFO, SoC etc.**

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DOI: 10.31838/ecb/2023.12.s1.157

I. INTRODUCTION

To accomplish the energy constrain related to highly complex digital system optimal network on chip (NoC) is predominantly used which can regulate the power management system [1-2]. In most cases highly complex dedicated wire connection are simplified with router design. On other side the demands for optimal methodology to narrow down power consumption are increasing steadily especially for compact electronic device models [3-4] such as mobile phone and other 5G related devices. The energy efficiency measures inadequacies inherent in existing NoC models systems have driven the development of new optimal router design for next generation ultralow power applications. In general the overall performance metrics for any NOC system component is largely depends on memory space model used to regulate the traffic flow. The major objective of high performance router design is to optimize the memory space requirement, avoid data congestion, and maximize the network reliability in each stages of data transmission between sources to destination. Among many network router models investigated [5], buffer less router is the most promising method used for energy efficient NOC design in digital systems and has proven to be an optimal technique well suited for reliable router interconnect over virtual channels interface. This reconfigurable NoC framework is organized as follows. Section 2 includes the detailed analyzes of exiting NoC routing models and FSM design techniques and various energy level optimization models used in memory less VC system and its VLSI hardware implementation. Section 3 discussed proposed configurable FSM based NoC architecture and associated power reduction techniques which includes optimal high performance data flow techniques Section 4 summarize the comparative analyzes of proposed NOC with existing NOC models through FPGA hardware synthesis. Section IV concludes the details.

The SoCs (System on Chips) are sophisticated devices that can include a variety of hardware accelerators as well as numerous processors for running software programmes. A growing number of FPGAs (reconfigurable architecture) are using networks on chip (NoC) as a solution to the issues associated with communication bottlenecks between IPs [1], [2], [3], [4], [5], and [6]. Several works have been suggested in order to boost the NoC's flexibility and runtime adaptation for reconfigurable IPs. The works in [7] and [8] specifically suggested a dynamically scaled NoC to add and remove routers in real-time. As seen in Fig. 1, routers are added to [8] in groups as sub-rows or columns. The suggested algorithms are put into practise using low-level HDL implementation in accordance with conventional handwriting. The low-level design approaches, however, are difficult and prone to mistakes. Runtime-scalable rows-and-columns-based NoC, Using a high-level modelling approach and unified modelling languages is one strategy to get over the design complexity and faults at the low level. One of the most promising methods for system development nowadays is known as model-driven engineering (MDE). In both industry and academia, UML is now the modelling language of choice.

In both industry and academia, UML is now the modelling language of choice. It was intended to function as both a general-purpose modelling language and a base for several domain-specific languages. One such area where UML extensions are needed to offer a more exact characterization of domain-specific phenomena is the field of real-time embedded software systems. As a result, the OMG is looking to create a new UML profile called MARTE (Modelling and Analysis of Real-Time and Embedded Systems) [9], [10]. Moreover, component-based architecture modelling and analysis as well as a range of computational paradigms have to be supported by MARTE (asynchronous, synchronous, and timed). In [11], [12], [13], [14], and [15], the

integration of IP-XACT with MDE-based UMLMARTE was shown.

First, the UML/MARTE is used to define the static and run-time scalable sub-NoCs at a high level. Following that, they are converted into an intermediate level of XML description that adheres to the IP-XACT standard.The reconfigurable rows and columns, as well as the entire top-level NoC's XML description, are then converted into VHDL. Lastly, the NoC HDL files are imported into Xilinx EDK to create the dynamically scalable NoC by combining with the reconfigurable IPs based on FPGA. By simulating a 3x3 NoC split into three components as a 2x2 static sub-NoC, a 2x1 reconfigurable column, and a 1x3 reconfigurable row, the proposed approach is shown to be valid.Once connected to the NoC routers, the entire system is implemented using a user-defined tiny IP address. It is seen as an excellent opportunity to get the most out of them by incorporating the reconfigurability notion into one of the most growing and trending design platforms, the NoC. The reconfigurable NoC's great flexibility and comprehensive customizability may pave the way for a fully adaptable NoC that can accommodate a wide range of benchmarks in accordance with runtime needs and requirements.The main goal of this effort is to present Dynamic Partial Reconfiguration (DPR) functionality to CONNECT Network-on-Chip (NoC) for Field Programmable Gate Array (FPGA) applications. It also examines how this reconfigurability affects network performance and how it might result in space and power savings. Dynamically reconfigurable applications are made fully customizable and more adaptable NoCs as a result of runtime reconfigurability. Dynamically reconfigurable NoCs outperform static NoCs in terms of area consumption by recycling some of the network area resources when they are not in use during runtime. A reconfiguration tool is created to assist the designer in selecting the best network configuration for each application. The minimum required throughput and the anticipated traffic load are inputs needed by the reconfiguration tool. The optimum network configuration and the smallest region that satisfies those requirements are determined using those inputs.

II. RELATED WORKS

In many digital systems different versions of NoC architecture is introduced to regulate the data flow and optimize the power dissipation which includes the optimal router design and reliability measures in detailed. In general NoC architecture comprises of FIFO based virtual channel (VC) [6] and crossbar switch [7] performance metrics are directly decides the overall system performance of NoC architecture. In most cases performance trade-off is unavoidable among these different NOC router design models. Implementation of FIFO based design model is applicable only with some energy level optimization models due to its parametric constraints.

In [8] investigates the various performance constrains in both buffered and bufferless reconfigurable NoC over XY routing algorithm. Here switching speed and Flexibility in selecting the direction for each port request are compared and deadlock is measured with 3x3 and 4x4 NOC router configuration. Finally performance metrics are analyzed which includes power, transmission latency and attainable data rate. In [9] proposed asymmetrical routing model for 3C NoC architecture using interleaved vertical edge routing algorithm. Here to maximize the system performance novel flit prioritization unit is introduced for bufferless mesh NoC. The results proved that the edge routing measure increased the system performance with least complexity overhead. In [10] analyzed probabilistic behavior of deflection routing and investigate the inherent statistical characteristics of the bufferless NoC. Here Markov chain models are incorporated to regulate the performance variation of bufferless router. The MC model is used to

formulate the network packet transmission distance based on hob distance [11] and applies flit deflection probability for reducing the performance degradation buffer less router and associated network reliability. In [12] developed optimized input/output buffer and cross bar switch using high performance priority encoder. Here path delay overhead that exists in Buffer fewer routers is optimally reduced using FSM based Arbiter design [13] and dynamic priority changes. Experimental results proved that the proposed router mitigate the Live/Dead lock problem and achieve 43% area efficiency.

In [14] developed three different buffer models for NoC router in SRAM design. To normalize the serial access mechanism and non-volatility characteristics of SRAM Domain-Wall Memory (DWM) is used as potential alternative to conventional SRAM. From the results it is well proved that the proposed network router offered significant area and energy efficiency of 36.1% and 55.1% respectively without compromising the network performance. In [15] router design is carried out using optimal 2D array buffers to hold transmission of packets during worst care data congestion. This array buffers allows multiple packet data forwarding with existing XY routing algorithm. By incorporating optimal path finding algorithm the overall packet congestion can be reduced with the proposed array buffer design. This array design is experimented with NoC architecture and results proved the superior system performance in terms of packet-delivery rate and network latency. In [16] introduced spin-transfer torque random access memory (STT-RAM) buffers to overcome the energy related issues that exists in conventional non-volatile SRAM based buffers in NoC design. As compared to other buffer models STT-RAM reduced the leakage power which maximize the overall network life time. By incorporating these optimal buffers units as virtual channels (VCs) the non linear variation in network dynamics is significantly reduced. System-on-Chips modelling using UML MARTE has been discussed in [14], [23], and [24]. Also suggested for IP administration is the integration of UML MARTE and IPXACT [25] in [26], [27], [28], and [29]. A specific network-on-chip work that uses UML-MARTE modelling to describe the NoC has been published in [30], [31], and [32]. A dynamically reconfigurable SoC using the UML/MARTE technique has also been put out in [33], [34], [35], [36], and [37]. The pieces in [33] and [37] serve as inspiration for our work. For modelling a system-on-chip that can be partially reconfigured, the authors provided a UML-IP-XACT method. They used MARTE to model the image processing IPs, which they then converted into IP-XACT before producing the files required for partial reconfiguration. As far as we know, there isn't a MARTE or IP-XACT strategy for creating a dynamically scalable NoC. Especially in studies pertaining to the NoC based on UML/MARTE, the NoC is regarded as a static topology and cannot be scaled up or down during run-time. The first are the connections between each router and the neighbouring IPs. The second links are those that link the east port routers in the second column with the west port routers in the reconfigurable column. The third set of links are those that connect to the top-most reconfigurable row by heading north. If the repetition of the links is defined, then links in the same direction are represented similarly to how routers are represented by a single model by a single link. From the south and west ports of the external routers, the 2x2 static sub-NoC is not connected to any router.Adjustable rows With the exception of a minor variation in the input/output ports, the models of the reconfigurable rows and the static sub-NoC are nearly identical. The models of every reconfigurable row, however, are comparable. The number of routers in the specified row will be the only variation. In order to connect east and west ports, the

router must repeat itself 164 times horizontally.

III. RECONFIGURABLE NOC ARCHITECTURE

The power dissipation in any NoC Technology is categorized into three type's namely a) Static b) Short circuit c) Dynamic. Among these three types the dynamic power dissipation plays vital role in the process of routing and data transmission which alone contributes roughly 90% of overall testing power consumption due to its statistical dependency with the circuit switching activity. In NOC routing the overall switching activity of directly depends on the transition characteristics of memory buffer module used for virtual channel. By reducing the memory size the digital transitions between two successive routers are controlled within some threshold limit. We are unaware of any MARTE or IP-XACT approach for building a dynamically scaled NOC. The NoC is considered to have a static topology in studies that use UML or MARTÉ, and it cannot be scaled up or down during runtime. The RSM profile, the MARTE HRM, and the UML component are essential entities for modelling the dynamically scalable NoC at the high level. Each reconfigurable row and column must be built as a component because the NoC is separated into dynamically reconfigurable sub-NoC that are arranged in independent reconfigurable areas and implemented as independent reconfigurable modules. This is a fundamental prerequisite for the execution of the DPR. Hardware resources are modelled using the HRM profile. It contains various extensions for simulating processors and hardware communication components. The RSM profile defines the multiplicity of the model and is used to simulate repeating structures. The NoC is a group of routers connected in a specific topology.

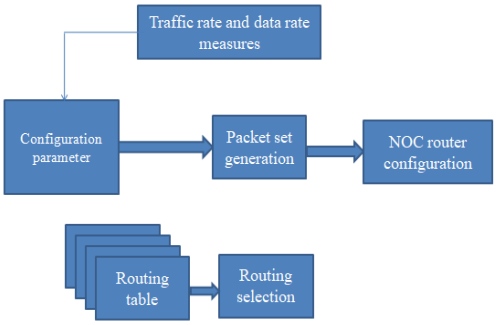

FIGURE 1. Proposed reconfigurable NoC architecture

a. Fsm Based Noc Configuration

Here finite state machine based parametric measures is used to configure the data flow and number of routers involved in overall NOC architecture at each virtual channel (VC) and associated FIFO mode as shown in Figure 1.

b. Hand Shake Protocols

In Hand shake protocol based NoC routing the FIFO based VC channel is replaced by two control signals namely valid and ready are controlled which explore the traffic condition and ports availability at the destination router. Here each router is equipped with handshake kind of data control protocol which is replacing FIFO based data connection with a virtual channel (VC). Here ready signal is used to assert the input and assert valid signal with the data port availability at the destination port. In FIFO based buffer channel the data transfer is enabled only when the two adjacent hand shake protocol valid and ready signals are high. Here both valid and ready signals are directly related to the request and acknowledgement signals in handshake protocols. TLS is an open standard that, like SSL, offers server authentication, data stream encryption, and message integrity checks, though there are some minor differences between TLS 1.0 and SSL 3.0 that prevent them from being interchanged. If neither party supports the same protocol, the parties must negotiate a common

protocol in order to communicate. The main objective of the TLS protocol is to provide privacy and data integrity between two communicating applications.

IV. RECONFIGURABLE NOC

In this section, the performance metrics of proposed memory less NoC router over conventional FIFO VC based NOC model and validated the metrics both in terms performance rate and switching activity control with associated energy efficiency measures. As compared FIFO based routing the proposed FSM handshake protocol based VC channels showed significant memory space reduction and power consumption rate with least possible hardware complexity overhead. The proposed NOC core is modeled using the Verilog HDL and synthesized using FPGA synthesizer for comparative analyzes as shown in Figure 2. The elastic buffer channel in NOC router offered flexible memory space tradeoff and tolerable error protection due to its controlled data flow.

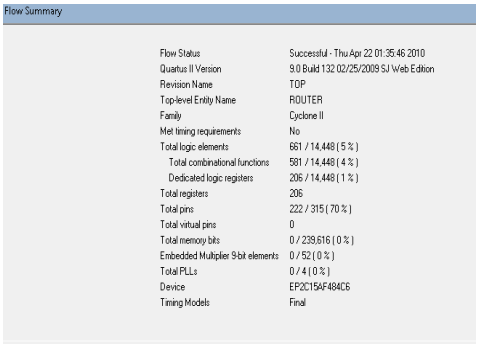

FIGURE 2. Hardware report summary

SIMULATION RESULT

In order to verify the functionality of the proposed FSM based NOC router model input stimulus is generated using exhaustive test bench with random input. Here 8x8 NOC router is configured using dedicated 64 dedicated IP blocks and associated router address. Based on high level FSM configuration 2x2, 3x3, 4x4 and 8x8 NoC is optimally configured using hand shake protocols are connected without using FIFO to regulate the data flow and queue the data input. Input packet comprise of both payload and destination address. During data routing destination address is processed and request is send in accordance with direction of data flow. Each router is equipped with the information link which can explore all nearest router and its port availability status. During port request in case of requested port is busy with other data transfer all received data is accumulated in virtual channels. Here round robin routing algorithm is used to allocate the priority to each direction irrespective to the frequency of request. With the inclusion of elastic buffer ports availability of destination router is estimated using signal assertion and transmission is begins accordingly.

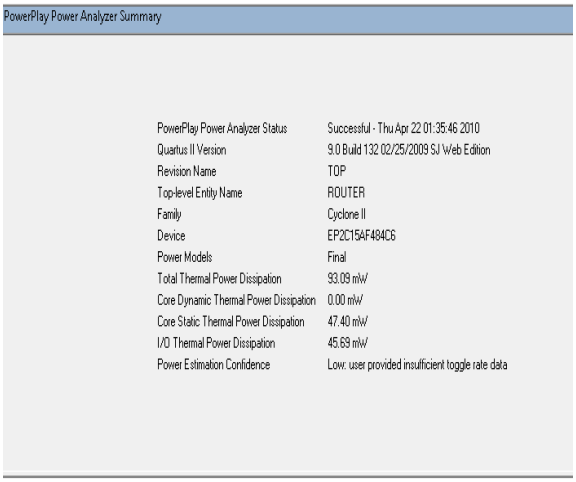

FIGURE 3. Signal transition report

TABLE 1. Performance comparison between FIFO based NoC vs. Hand shake protocol based NoC router design

NOC model	Area(LE's used)	Memory used
Existing router	583	2560
Memory optimized router	661	NIL

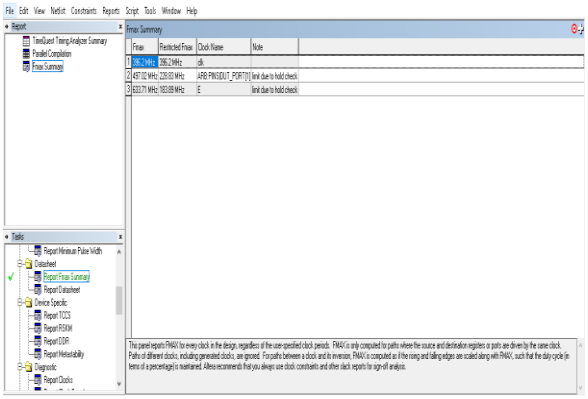

FIGURE 4. Performance Efficiency report

The efficiency of power optimization through data transition reduction scheme is analyzed using dynamic power management (DPM) in terms of both digital transition reduction and associated dynamic power consumption reduction as shown in table 2. To illustrate the energy efficiency during the evaluation of signal constellation post simulation has been carried out which will generate the value change dump (.vcd) file. The dynamic digital transitions during iterative computation and associated switching activities are note down for energy measurements. The power play power analyzer tool is used to compute the overall power dissipation which includes both static and dynamic power as shown in table 2

TABLE 2. Performance comparisons of proposed dynamic efficiency as compared to convention FIFO based NOC model.

NOC model	**Fmax (MHz)**	**Power dissipation (mW)**
Existing NOC	343.17 MHz	93.17mW
Proposed dynamic configuration NoC	396.2 MHz	93.09mW

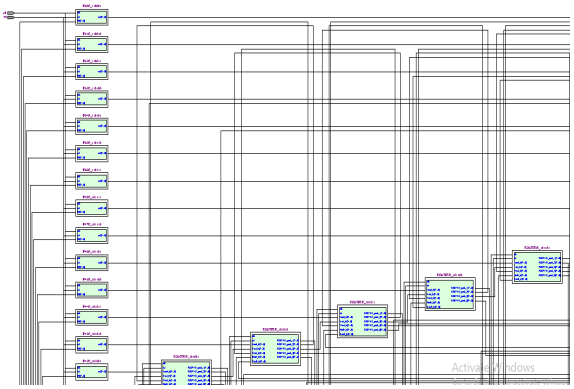

FIGURE 5. RTL schematic view

V. CONCLUSION

Here in this paper FSM based configurable memory less VC based NoC architecture is presented for dynamic configuration for highly complex network interconnection within the chip. Here hand shake protocol is used to regulate the data flow without using FIFO based VC to formulate the communication information link for high rate data transfer. Here, in proposed memory efficient NOC router architecture data buffering is completely stopped using valid and request signal as duplex communication channel and one controller to assert control signals. By selecting parameters NOC configuration and associated routers are interconnected. From the hardware synthesis results it is well proved that the proposed memory less NOC offered improved energy

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