SIMULATION OF SINGLE GATE MOS CAPACITOR USING MOSCAP WITH P+ POLYSILICON AND N+ POLYSILICON TYPE GATE ELECTRODES FOR ESTIMATING THE CAPACITANCE

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Abstract

Aim: The aim of this research work is to determine the simulation of a single gate MOScapacitor using “MOScap " with p+ and n+ polysilicon type gate electrodes for estimating the capacitance.
Materials and Methods: Data collection containing estimation of capacitance from the nanohub website was used in this research. Samples were considered as (N=20) for p+ polysilicon and (N=20) for n+ polysilicon in accordance with the total sample size calculated using clinical.com.
Results: Comparison of capacitance is done by independent sample test using SPSS software. There is a statistical indifference between p+ polysilicon and n+ polysilicon. p+ poly silicon (3.7629%) showed better results in comparison to n+ polysilicon (3.2053%) where the p value is insignificant ($p=0.673, p>0.05$).
Conclusion: p+ poly silicon appears to give better capacitance than n + polysilicon to estimate capacitance.

Keywords: Single gate, MOScapacitor, p+ polysilicon, n+ polysilicon, Nanohub, Novel simulation MOScap tool.

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1. Introduction

A capacitor is a device used to store electric charge. In its easiest structure, it comprises a couple of conductors isolated by a cover (dielectric material)(Lindsey and Kalkur 2000). MOScap is the MOS (metal oxide semiconductor) capacitor that is a two terminal gadget which comprises three layers (Hu 2010). The primary reason to study MOS capacitors is to understand the principle of operation as well as become familiar with some of the routinely used characterization techniques for MOS field effect transistors (MOSFETs)(Pantelakis 1991). The Novel simulation MOScap tool on nanohub.org simulates the one-dimensional electrostatics in single and dual-gate MOS device structures (Ciucu 2005)along the growth direction as a function of device dimension, oxide charge, temperature, doping concentration, and AC frequency (Taur and Ning 2013).

About 125 Google Scholar and 172 ScienceDirect articles were seen related to this work carried out in the last few years. The main importance of this work is that shallow n+ and p+ junctions that are fabricated using a “spin -on” dopant are introduced into the material and activated by irradiation (Khan, Ahmed, and Ali 2016). This study promotes green technology by MOScapacitor SiC-based hydrogen sensors represent a class of unique materials due to their electronic charge transport properties when compared to conventional covalent semiconductors such as silicon(Lipovsky, Gedanken, and Lubart 2013).Polysilicon is used in a variety of VLSI manufacturing processes. One of its most common applications is as a gate electrode material in MOS devices (Rahaman, Chattopadhyay, and Chattopadhyay 2012) .The electrical conductivity of a polysilicon gate can be increased by depositing a metal (such as tungsten) or a metal silicide (such as tungsten silicide) on top of it.(Tan and Hwu 2015).

Our team has extensive knowledge and research experience that has translated into high quality publications (Vickram et al. 2022; Bharathiraja et al. 2022; Kale et al. 2022; Sumathy et al. 2022; Thanigaivel et al. 2022; Ram et al. 2022; Jothi et al. 2022; Anupong et al. 2022; Yaashikaa, Keerthana Devi, and Senthil Kumar 2022; Palanisamy et al. 2022). The unanswered problem in this MOScap is the problem of using non-linear capacitors in a linear system on a chip. The capacitance–voltage (C–V) technique of estimating gate oxide thickness, substrate doping concentration, threshold voltage, and flat-band voltage is a potent and widely used approach. Main aim of this research is to perform the simulation of a single gate MOScapacitor with p+ and n+ polysilicon using the Novel simulation MOScap tool for estimating the capacitance.

2. Materials and Method

This study was carried out at the Simulation laboratory, Saveetha School of Engineering, Chennai. The sample size calculation was done using previous study results (Jayant Baliga 2006) using clinical.com by keeping alpha error-threshold by 0.05, enrollment ratio as 0:1, 95% confidence interval, power at 80%. Group 1 and Group 2 are p+ polysilicon (N=20 study group) and n+ polysilicon (N=20 control group) respectively. The total sample size was 40.

Sample preparation for two groups was done by collecting 40 dataset samples, 20 for each group. In this work the proposed simulation tool is MOScap. The simulated data are collected from nanohub.com to measure the capacitance of p+ polysilicon and n+ polysilicon.

Testing is done by installing a MOScap tool from nanohub.org. Select the type of gate electrode in the Novel simulation MOScap tool. Apply the thickness of the gate insulator and semiconductor by keeping model parameters like (fixed charge density in gate insulator and interface charge density in gate insulator) as a constant, select the parameter and run the simulation to get the graph.

Statistical Analysis

The capacitance comparison of p+ polysilicon and n+ polysilicon was done using IBM-SPSS software. Since the variables were independent of each other, an independent sample t-test was done for estimating the mean capacitance.

3. Results

In this research work of estimating the capacitance, both the p+ polysilicon and n+ polysilicon produce the results with insignificant value 0.673. It is observed in fig. 1 the mean capacitance of p+ polysilicon is more compared to n+ polysilicon. In this investigation p+ and n+ polysilicon both the electrodes appear to produce the same variable results with capacitance. It is observed in fig. 1, the mean capacitance of p+ polysilicon is more compared to n+ polysilicon. Figure 2 represents the predicted output graph obtained by the p+ polysilicon and fig. 3 represents the predicted output graph obtained by the n+ polysilicon.

The p+ polysilicon had the highest mean capacitance, 3.7629% in comparison to n+ polysilicon 3.2053%. The descriptive statistics in Table 1 demonstrated that p+ polysilicon had less error rate than the n+ polysilicon. Table 2 represents the mean value, std.difference, std.error difference.

There appears to be a statistically insignificant difference ($p=0.673$,$p>0.05$) in both the methods using independent sample t-tests. These results showed that p+ polysilicon can be used to predict capacitance at a faster rate in comparison with n+ polysilicon .To simulate the single gate MOScapacitor for the purpose of estimating the capacitance sample t-test. This result shows that p+ polysilicon is insignificant better than n+ polysilicon.

4. Discussion

This research work of predicting the capacitance in p+ polysilicon had the highest mean capacitance (3.7629 F) in comparison to n+ polysilicon (3.2053 F). There appears to be a slight increase in the significant difference but it is statistically insignificant. In p+ polysilicon it is the easiest and cheapest way to determine the capacitance. Related works carried out during recent years (Xia et al. 2017) have less capacitance than the proposed p+ polysilicon (Khan, Ahmed, and Ali 2016).

MOScap simulates the one-dimensional electrostatics in typical single and dual-gate MOS device structures along the growth direction as a function of device dimension, oxide charge, temperature, doping concentration, and applied frequency(Tan and Hwu 2015). Among the quantities simulated, the low and high-frequency capacitance-voltage (CV) characteristics and various spatial profiles (e.g., energy band, vertical electric field, charge densities etc.) are of special importance (Khan, Ahmed, and Ali 2016).MOSCap also has an option for plotting the semiconductor surface potential as a function of applied gate potential(Yang et al. 2021). In the following, we describe the input parameters, the output quantities, and important information that can be extracted from these outputs using the MOScap tool. Factors affecting the capacitance are Shallow n+ and p+ junctions are fabricated using a “spin-on” dopant introduced into the material and activated(Pulfrey 2010).

MOScapacitors are expected to lead to a significant improvement in the future. In future it will act as an excellent tool in high end uses.The fundamental problem of such gate capacitors is their high voltage dependency, which is caused by charge distributions that differ in the accumulation, depletion, and inversion regions.

Scalability and retention are provided by an ultra-thin oxide-nitride-oxide (ONO) layer with high trap density and strong localisation of the trapping in the SONOS memory. Longer retention with thinner tunneling dielectrics may be possible, resulting in lower operating voltages. However, for high-speed performance, SONOS needs to enhance erase time, which is the process of releasing electrons from the traps.

5. Conclusion

In this study, estimation of the capacitanceisdonebyNovel simulation MOScap tool.The capacitance of p+ polysilicon (3.7629 F) that operates using nanohub appeared to give better results when compared to the capacitance of n+ polysilicon (3.2053F).

Declaration

Conflict of Interests

No conflict of interest in this manuscript.

Authors Contribution

Author VBB was involved in data collection, data analysis, and manuscript writing. Author SCK was involved in conceptualization, data validation, and critical review of manuscripts.

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Tables and Figures

Table 1: Capacitance for p^+ polysilicon compared by gate insulator thickness

S.NO	**GATE INSULATOR THICKNESS (μm)**	**CAPACITANCE (F,10^{-8})**
1	0.1	3.84000
2	0.2	3.70044
3	0.3	3.53407
4	0.4	3.43769
5	0.5	3.38813
6	0.6	3.13538
7	0.7	3.11901
8	0.8	3.10945
9	0.9	2.96989
10	1.0	2.92035
11	1.1	2.10395
12	1.2	2.0709
13	1.3	1.97121
14	1.4	1.47326
15	1.5	1.30659
16	1.6	1.10659
17	1.7	0.93992
18	1.8	0.59782
19	1.9	0.47698
20	2.0	0.26890

Table 2: Capacitance for n^+ polysilicon compared by gate insulator thickness

S.NO	**GATE INSULATOR THICKNESS (μm)**	**CAPACITANCE (F,10^{-8})**
1	0.1	3.47732
2	0.2	3.4192
3	0.3	3.30309
4	0.4	3.18694
5	0.5	3.01271
6	0.6	2.89656
7	0.7	2.78041
8	0.8	2.60618
9	0.9	2.49003
10	1.0	2.3158
11	1.1	2.25773
12	1.2	2.0835
13	1.3	1.96735
14	1.4	1.67697
15	1.5	1.5027
16	1.6	1.21992
17	1.7	0.9659
18	1.8	0.7557
19	1.9	0.5656
20	2.0	0.1789

Table 3: Comparison of mean and capacitance using p+ polysilicon and n+ polysilicon .

Parameter	**Group**	**N**	**Mean**	**Std. Deviation**	**Std. Error Mean**
Capacitance	p+ polysilicon	20	3.7629	1.00568	0.22488

	n+ polysilicon	20	3.2053	0.96825	0.21651

Table 4: Independent sample t-test in estimating the capacitance of p+ polysilicon and n+ polysilicon. There appears to be a statistically insignificant difference($p>0.05$) in both the methods.

Parameter	**Equal Variances**	**Levene's Test for Equality of variances**		**T-test for Equality of Means**	
		F	Sig	t	df
Capacitance	Assumed	0.181	0.673	1.786	38
	Not assumed			1.786	37.945

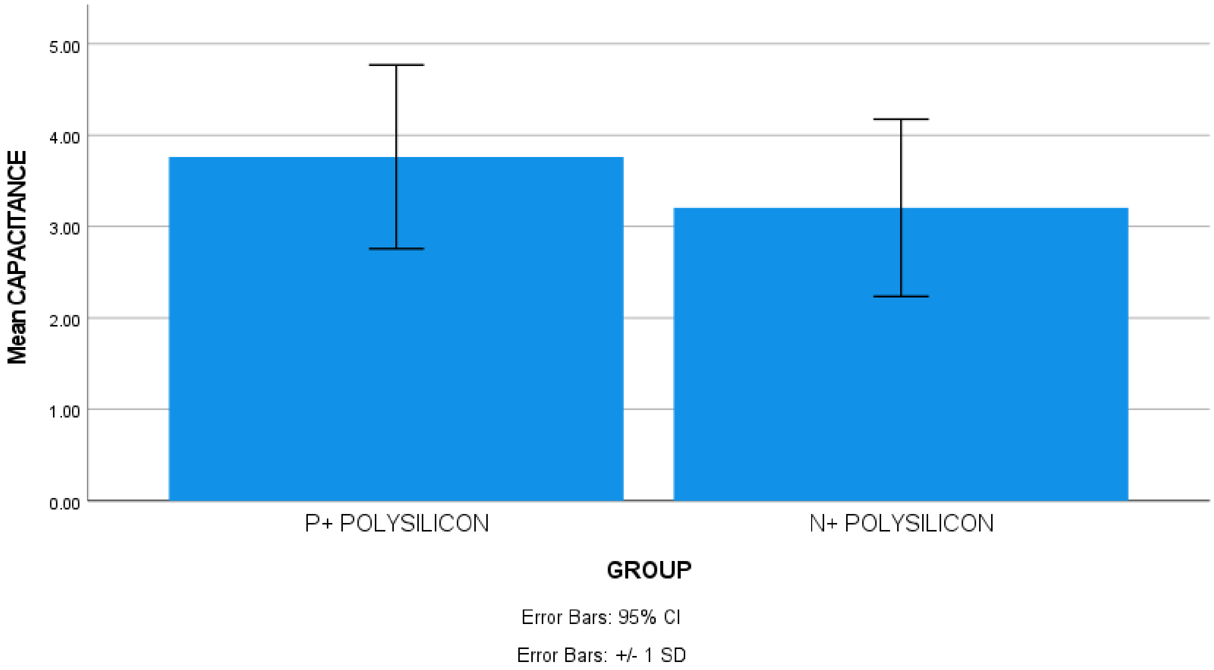

Fig. 1: Bar chart estimation of capacitance of p+ polysilicon and n+ polysilicon. Both comparisons appear to produce the same variable result with capacitance ranging from 0.32% to 0.37% X axis.p$^+$ polysilicon and n+ polysilicon Y axis. Standard Deviation is ± 1.

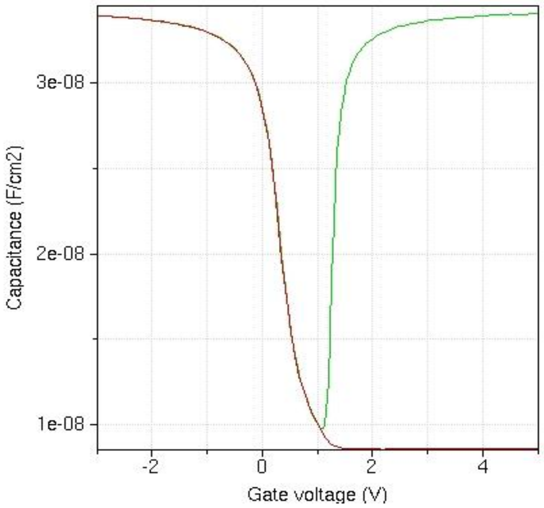

Fig. 2: Graphs represent the outcome of the capacitance of p+ polysilicon using the MOScap Tool in nanohub.org. Red line represents low frequency and green line represents high frequency.

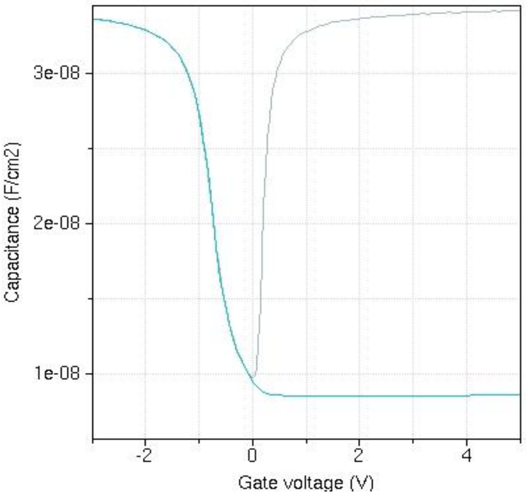

Fig. 3: Graphs represent the outcome of the capacitance of n+ polysilicon using the MOScap Tool in nanohub.org. Skyblue line represents low frequency and blue line represents high frequency.