LOW NOISE AMPLIFIER PERFORMANCE ENHANCEMENT BY INCORPORATING STABILIZATION AND INPUT-OUTPUT COMPONENTS MATCHING DESIGN FOR LOW ENERGY TECHNOLOGY APPLICATIONS

Shinjini Yadav[1], Saima Beg[2]

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Abstract:

Since the scalability of technology has gotten smaller, highly integrable, and more accessible, complementary metal-oxide-semiconductor (CMOS) technology has gained popularity in wireless applications. Wireless technology has become widely used in recent years, not just for consumer gadgets but also for medical sensors like body temperature and heart rate monitors. This new trend of fast information monitoring employing portable and wireless devices has adopted low noise amplifier for low energy technology. The objectives followed in the proposed research article are, analysis of recent trends on LNA requirements and designs study through literature survey and finalizing LNA topology and specifications from the chosen band (spectrum) of application.

Keywords: LNA, stabilization, I/O matching, low energy technology

[1,2]Integral University, Dept. Electronics & Communication Engineering, Lucknow, India

Email: [1]yadavshinjini@gmail.com, [2]saimabeg@iul.ac.in

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1. Introduction

The proliferation of wireless standards and the development of dynamic standards and applications, such as software-defined radio, are driving the demand for the next generation of wireless devices that combine a number of standards into a single chip-set to provide a wide range of services. Reconfigurable multi-standard portable devices are desirable, and hardware should be shared and reused as much as possible to reduce device costs and footprint. This study suggests a number of cutting-edge circuit topologies that are appropriate for multi-standard applications and can satisfy diverse standards at low cost. This research paper proposal would concentrate on the important aspects listed below:

1. Generic challenges to the modern RF/Wireless systems and solutions
2. Design aspects and challenges in RF-CMOS Integrated Circuits
3. LNA and RF-Mixer

A thorough understanding of low-power design at the component, circuit block, and sub-system levels (such as receiver, transmitter, and PLL), and system levels are necessary for wireless RF systems, such as RF-Mixed-Signal System-On-Chip systems, to use less power. This paper's fundamental spotlight is on power utilization advancement for remote RF IC circuits.

Getting the cost of the localization function down is another difficult task for wireless sensor nodes with wireless localization. The cost of each wireless sensor node must be kept to a minimum because most applications require a large number of them. A standard CMOS technology is used to cut costs because it is best suited for large-scale manufacturing. A methodical plan and thorough layout can also reduce the cost of a particular system. A straightforward but practical system architecture could help to cut costs and power consumption.

RF Receiver Chain and LNA Design Aspects

After LNA, a down-conversion mixer converts an incoming RF signal to the intermediate frequency (IF), depicted in Figure 1, a low frequency. The IF stage's frequency in the direct conversion design begins from DC. Because it provides strong isolation between the RF stage and the IF stage by employing distinct frequencies, the IF stage makes it easier to achieve the necessary high gain and high stability in RF receivers.

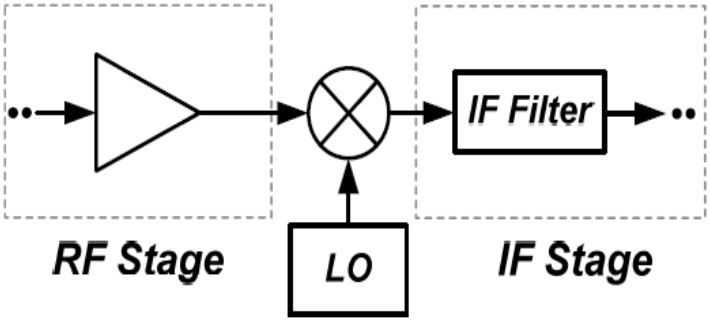


Figure 1: Block diagram of a mixer in RF architecture consisting LNA and mixer

The BLE front-end receiver circuit's (LNA) initial stage is the low noise amplifier. Geographies, input matching organizations, source degeneration criticism circuits, biasing circuits, and result matching organizations are the five parts that make up a LNA design. The 45 nm processing method from the generic processing design kit (GPDK) was used to create the circuit. In order to construct an LNA correctly, it is also necessary to comprehend performance characteristics and the RLC circuit theory.

Modern IC technologies' high levels of integration make it possible to include additional passive components like inductors on a chip, making it possible to achieve the goals of efficient RF CMOS. Also, as the new design technologies use lower device sizes, the transmission line effects won't be as bad as they were with the previous technologies. These elements aid in overcoming the difficulties of integrating direct conversion receivers into a single integrated circuit. Due to the following four issues, this architecture hasn't been used as much as it could have:

- I/Q mismatch
- DC offsets
- Flicker noise
- Even order distortion

The fundamental components of portable wireless communication devices are radio frequency integrated circuits (RFICs). One of the greatest technologies for implementing RF front-ends is

CMOS technology. The following characteristics, such as cheap cost, constant device scaling, and high integration, make this viable. The operating frequency is shifting towards the 5GHz band as a result of an increase in demand for consumer electronic services. This implies that the introduction of novel RF front-end designs is desirable.
LNA is a key component in a typical design because it determines the sensitivity of the entire system. Hence, it should satisfy a number of performance constraints. Input impedance of 50 ohms must be steady, noise figure must be low, and other stages' noise must be suppressed with high gain.

MOSTs biassed in the weak/moderate inversion area are used to achieve low thermal noise, and chopper stabilisation is used to shift 1/f-noise out of the signal band to ensure overall low noise performance.

Literature Survey
Kai-Chun Chang et al., (2020) [10] introduce a low-power CMOS low clamour enhancer (LNA) operating at 17.7-42.9 GHz for radio cosmic benefits in 65-nm CMOS innovation Based on a few data transmission upgrade methodologies, The proposed LNA produces a big commotion figure and a high increase across a wide recurrence range while using little power. The LNA is a tool that can help you achieve your goals. In the 3-dB data transmission capacity range of 17.7 to 42.9 GHz, the peak rise is 20.1 dB, and the commotion figure (NF) is between 2.8 and 4.3 dB. At 28GHz, this method uses less than 18 mW of dc power and has an OP1dB of 2.2 dBm. The figure-of-merit (FOM) for this study is 19 GHz/mW, highlighting the importance of distributed K-band and Ka-band LNAs. The chip's overall area, including padding, is 0.45 mm2.

Low commotion speaker plan and execution research of collector RF front-end for narrowband remote interchanges was introduced by Amgothu Laxmi Divya et al., (2020) [11]. The LNA is the distant collector's focal structure square. For reconfigurable applications like Wireless LAN, a single final cascode CMOS LNA is designed. This original copy's purpose is to plan an LNA fitting for remote applications with more refined execution measurements. The goals of this project are to use an inductive degeneration normal source stage to achieve sound decrease and high increase. The proposed LNA covers the full reenactment and resulting in a 2.44GHz recurrence band. Be that as it may, the ideal info and result coordinating organization is accomplished with appropriate converse protecting and fantastic security.

The body drifting and self-inclination technique was proposed by Jin-Fa Chang et al. (2021) [12], in which the semiconductor's body is related with its channel by an opposition (13.6 k in this work). The approach for sub-6 GHz 5G frameworks is accounted for by a low-power 3-9 GHz CMOS low-commotion enhancer (LNA). Because of the forward body-to-source inclination (VBS) (for example, minimal edge voltage Vth) and the semiconductors being liberated from the substrate spillage, the LNA's S21 and commotion figure (NF) improve. These are among the lowest power esteems yet observed for CMOS LNAs with data transmission larger than 6 GHz and NF less than 3.5 dB, according to the creators.
They demonstrate body drifting and self-inclination in a 3-9 GHz CMOS LNA. The LNA has improved in S21 and NF as a result of forward-one-sided VBS (such as tiny Vth) and semiconductors released from substrate spillage. Low PD is attained because low VDD of 1 V or 0.8 V is relevant due to low Vth. The LNA's well-known LP and LN performance (NF of 2.89 dB at PD of 3.3 mW, for instance) demonstrates its suitability for 5G networks operating at frequencies below 6 GHz.

Sakshi Singh Dangi and coworkers, 2021) [13] planned the RFIC (Radio Frequency Integrated Circuit) with CMOS (Complementary Metal Oxide Semiconductor) technology. Along with Bluetooth, Worldwide Interoperability for Microwave Access (Wi-MAX), and Wireless Fidelity Local Area Network (Wi-Fi LAN), CMOS technology is gaining traction in the business world. Utilizing Complementary Metal Oxide Semiconductor (CMOS) technology to construct RFICs offers significant advantages in terms of speed and cost. Additionally, CMOS technology permits a greater degree of small inclusion on a single chip. This is how CMOS is thought of at its core. It is frequently used in development of very large scale integration (VLSI), where hundreds to thousands of semiconductors can be coordinated on a single chip or bite the dust. RF designers gain even greater value from CMOS's quick working utility. With incredible phases of coordination on a single chip, these advantages enable CMOS innovation to function effectively within the GHz recurrence range, delivering superfluous execution at a low cost. On CMOS, it's a no-brainer innovation decision because of today's virtual broadcast communications and the need for high flagging rates in the most such portion of the radio spectrum.

2. Methodology

It is desired to combine various standards into a single chip-set in order to decrease power consumption, free up space, and improve the competitiveness of this new product. The frequency spectrum for several standards is displayed in Figure 3. Two conclusions can be drawn:

- The terms "signal power" and "frequency bands" are defined differently in each standard;
- Many channels could enter the collector with next to no pre-separating, going about as in-band obstructions and making serious contortion.

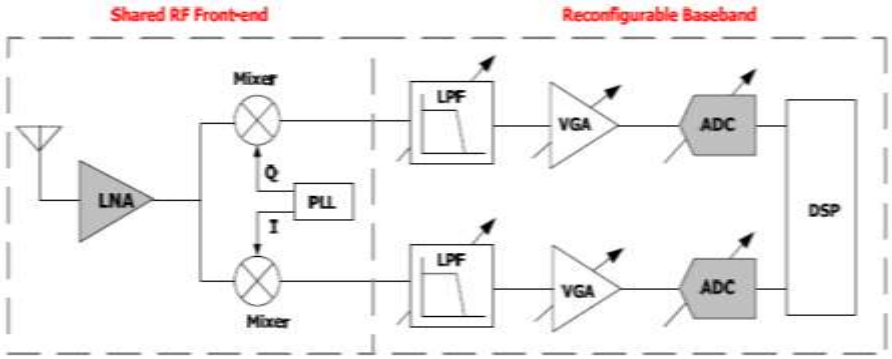


Figure 2. A down-conversion MIXER-based reconfigurable direct conversion receiver is depicted as a block diagram.

Based on these data, two major difficulties may be recognised for the design of RF-Down-conversion mixers:

Before examining several radio receiver architectures, a few of their particular issues are initially explained. In wireless communication, several frequency spectrum frequencies are shared by virtually an infinite number of users. Thus it's conceivable for powerful signals to coexist with weak ones in close proximity. An RFIC radio receiver must be able to identify the desired signal and reject all interference by making use of imperfect active and passive components. There are two main issues with the receiver design:

- Rejection of images
- Range of motion.

The receiver needs to be able to select the required signal from among the many other signals in the spectrum. In the best case scenario, a bandpass filter with a bandwidth as wide as a channel and a center frequency set at the required RF signal can accomplish this goal.

The primary factors that determine a receiver's dynamic range are the noise figure, the LNA's nonlinearity, and the first mixer. If the targeted RF signal is weak and surrounded by strong interferers, the preselection RF band pass filter cannot block unwanted signals. These huge interferers might overpower the resulting IF circuits and prevent the handling of the ideal sign in the wake of being enhanced in the recipient's front-end blocks (LNA and blender). In addition, these significant interference sources distort the receiver's signal-to-noise ratio (SNR), which raises input referred noise.

Additionally, due to nonlinearities in the LNA and mixer, some of these powerful interferers' intermodulation distortions may fall on the intended channel after down conversion. Because the IF filter cannot tell the difference between these undesirable signals and the required IF, these distortions behave like noise.

A valid defence would be how to achieve the target of the given goals (covered in parts later) in a professional cum technical way. A wireless receiver architecture for reconfigurable direct conversion is shown in Fig. 3 (in the section above).

The major design of the work (the LNA circuit) can be served by using parallel narrow band receiver routes with band selection switches, however this method is more expensive, takes up more space, and uses more power. A highly linear broadband RF front-end with changeable baseband blocks that can satisfy various requirements with minimal hardware implementation is a more adaptable and cost-effective option for reducing silicon size and power consumption.

There are numerous circuital designs that need to be simulated and analysed in order to approach a design that is being targeted for the low power and high speed characteristics. A powerful Circuit simulator tool will be needed to achieve the goal. The list of some such tools is provided below:

Simulator environment: SPICE (schematic level)
• HFSS and SPICE software from Keysight Technologies' Advance Design System

Adoption of technology nodes:
• CMOS (Level 49 and above) (Level 49 and above)
• Either 130 or 180 nm (Low voltage node)

The planned research project aims to follow the following objectives:

- By a literature review, current trends and analyses on LNA requirements and designs will be examined.
- Establishing the LNA's final topology and requirements for the application's chosen band (spectrum).
- Finalizing the schematic topology according on the application and technology (RF-CMOS here at 65 or 130 nm).
- Planning and modelling the performance of the LNA in a real RF environment.
- Verification and adjustment of the design to meet the specifications. (Publishing the conventional and original findings found in credible journals).

3. Results and Discussion

Amplifier with stabilization components added

A chopper is used to stabilize the amplifier and eliminate offset and flicker noise. A ripple reduction loop (RRL) is intended to eliminate the ripple caused by up-modulating offset and flicker noise. The RRL operation's notch in the overall transfer function is eliminated when a multi-path architecture employing both a low-frequency path (LFP) and a high-frequency path (HFP) is implemented. The low frequency path amplifier is implemented using the RRL and the chopper method. The high-frequency path amplifier utilizes a class-AB output stage to improve power efficiency. The system exhibits a first-order frequency response due to the transfer functions of the LFP and HFP, which are compensated for by nested Miller. The low-noise multi-path amplifier was made with a 0.18 m 1P6M complementary metal-oxide-semiconductor (CMOS) technology. The recommended low-commotion functional intensifier has a functioning area of 1.18 mm2 and a power utilization of 0.174 mW with a 1.8 V stockpile. The suggested low-noise amplifier has an input referred noise of 11.8 nV/Hz, a unit gain bandwidth (UGBW) of 3.16 MHz, and a noise efficiency factor (NEF) of 4.46.
The external source impedance has been set to 50 Ohms, and a matching network has been attached to the input. Hence, the conjugate of S22 will be the ideal load reflection coefficient given that the input matching network is fixed.

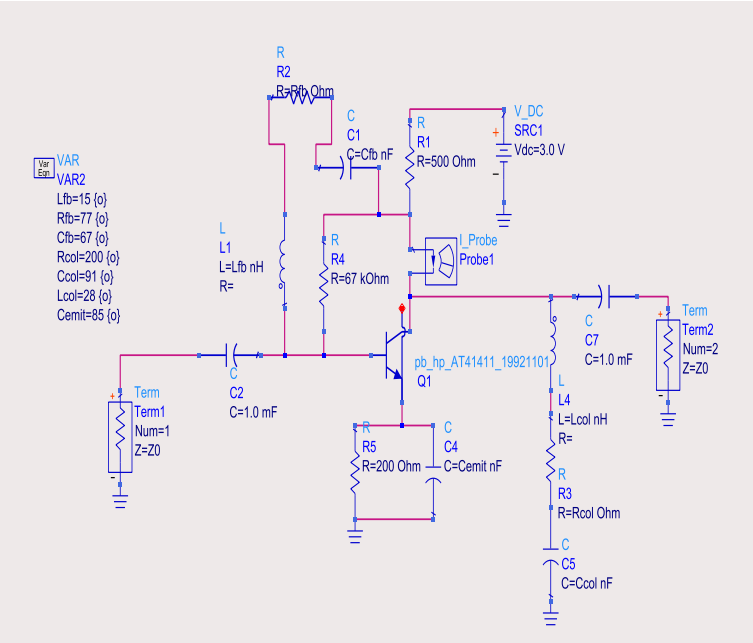


Figure 3: Amplifier with stabilization components

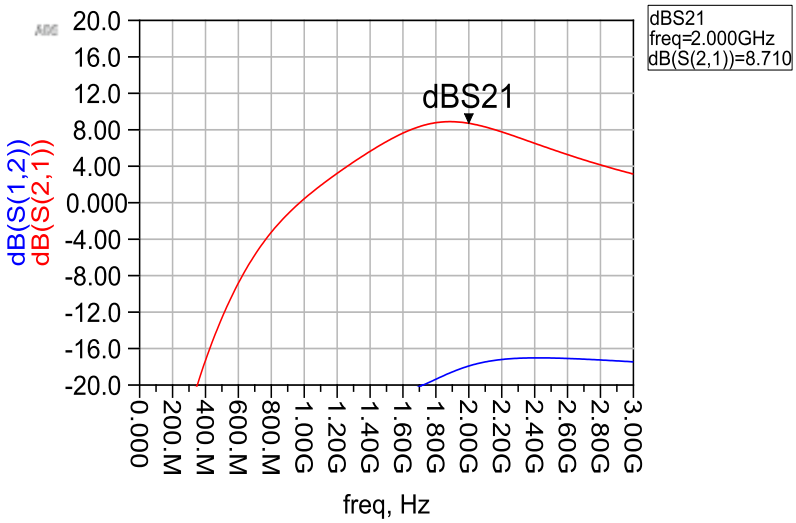


Figure 4: Frequency response of amplifier gain

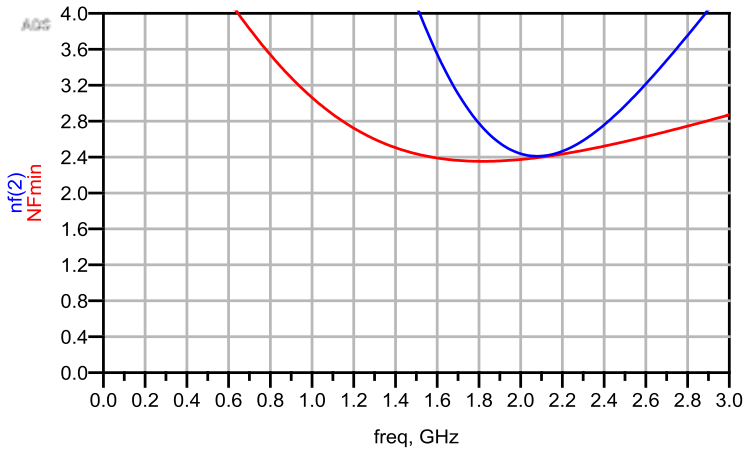
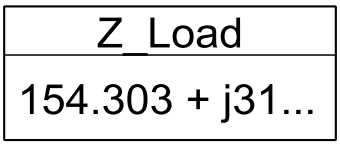


Figure 5: Noise efficiency factor response



Optimization of amplifier input and output matching networks for gain,input match, output match, and noisefigure.

There have been several LNA circuits in RF CMOS shown in earlier years, but there haven't been many precise design techniques for extremely low noise figures. In many situations where linearity is valued more than noise figure, noise figure is somewhat sacrificed due to the trade-off between linearity and noise figure. Nonetheless, it is conceivable to have strong linearity and noise performance, and this will be covered in more detail later in this paper. Because the LNA dominates the receiver's overall noise figure, nearly all techniques are based on optimizing noise performance through preset gain and power dissipation. In the interim, the other parameters are tailored to the requirements of the numerous uses they serve through interactive and simulation methods.

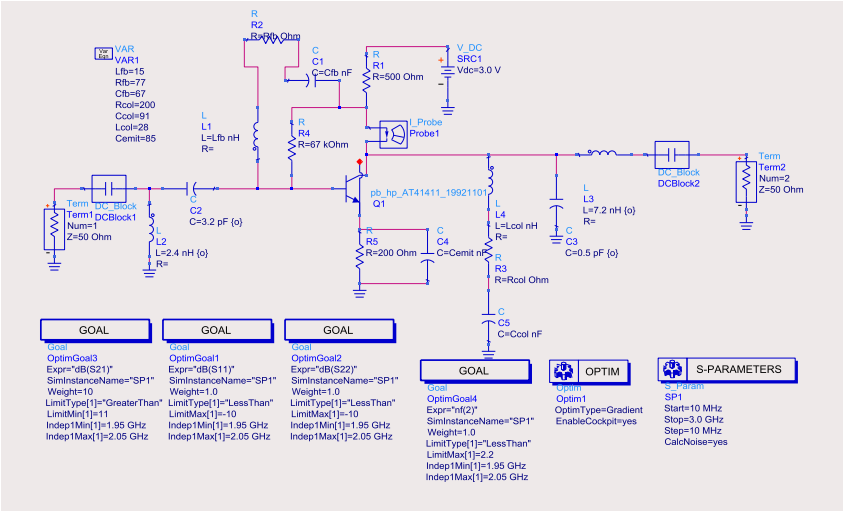


Figure 6: Amplifier with input and output matching networks

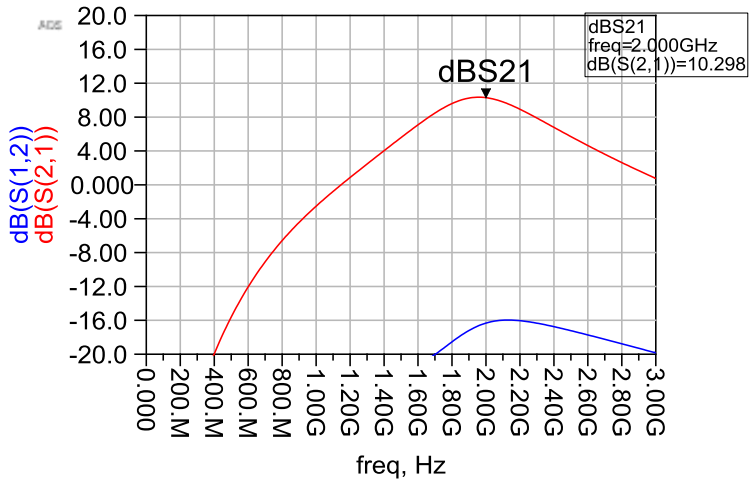


Figure 7: Frequency response of Amplifier with input and output matching networks

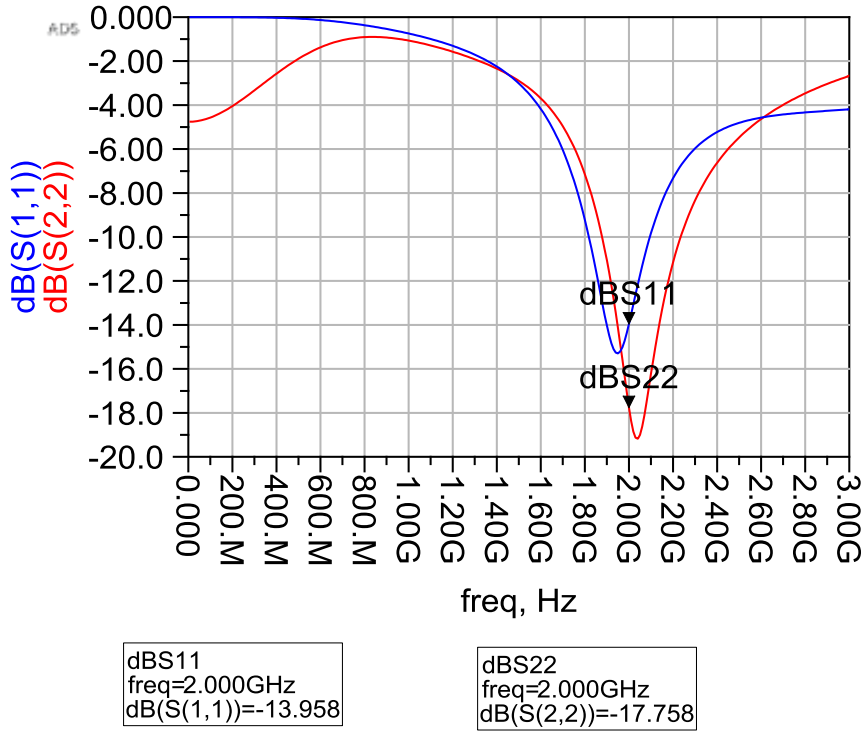


Fig 8: Amplifier with stabilization, input, and output matching components added

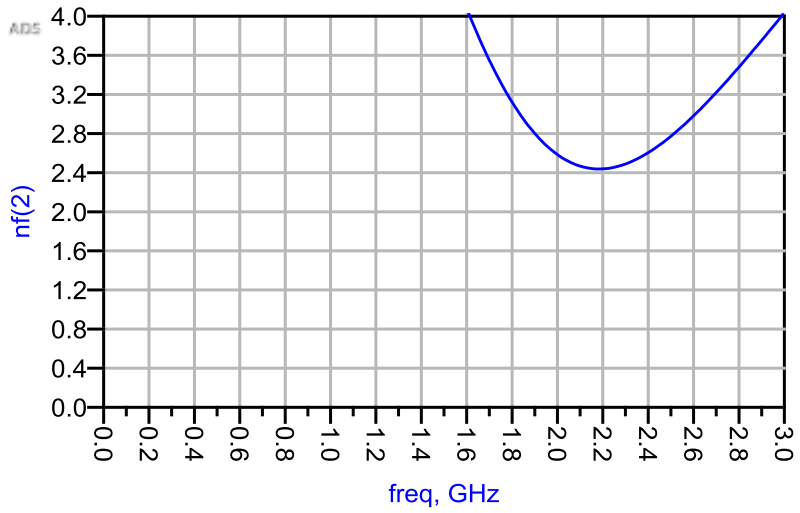


Figure 9: Noise efficiency factor response of Amplifier with input and output matching networks

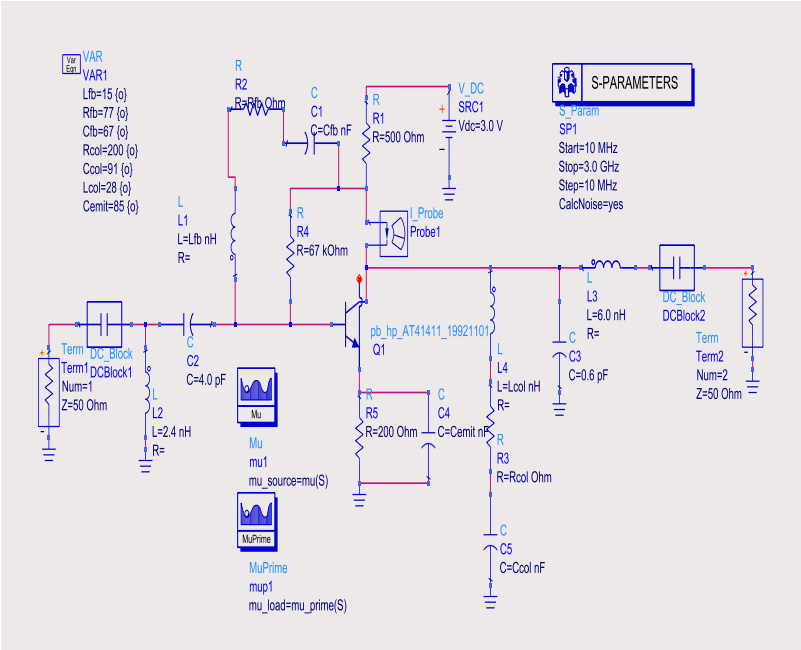


Figure 10: Amplifier with stabilization, input, and output matching components added

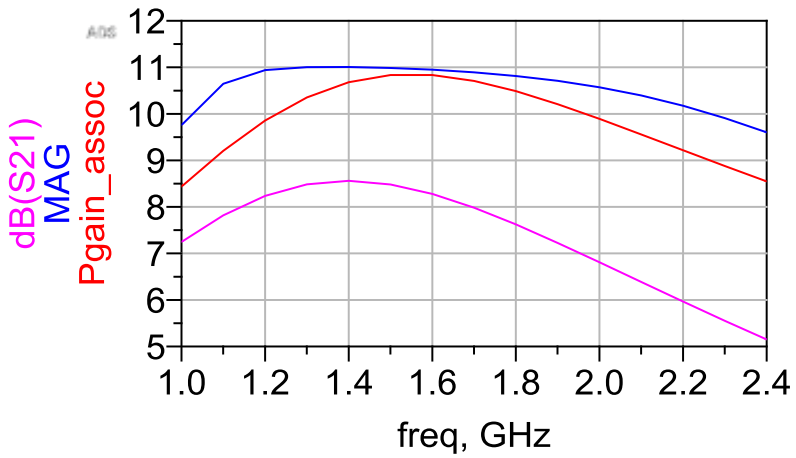


Figure 11: Frequency response of amplifier with stabilization, input, and output matching components added

Highest available gain, corresponding power gain (input and output are then conjugately matched for NFmin), and dB (S21). Using Z0 Ohm terminations, the minimum noise figure, dB, and noise figure.

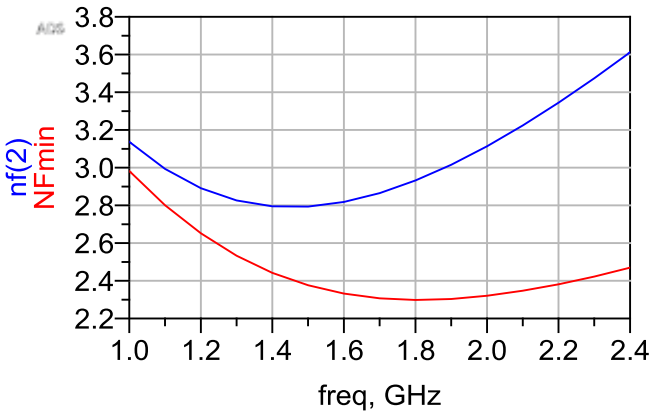


Figure 12: Noise efficiency factor response of amplifier with stabilization, input, and output matching components added

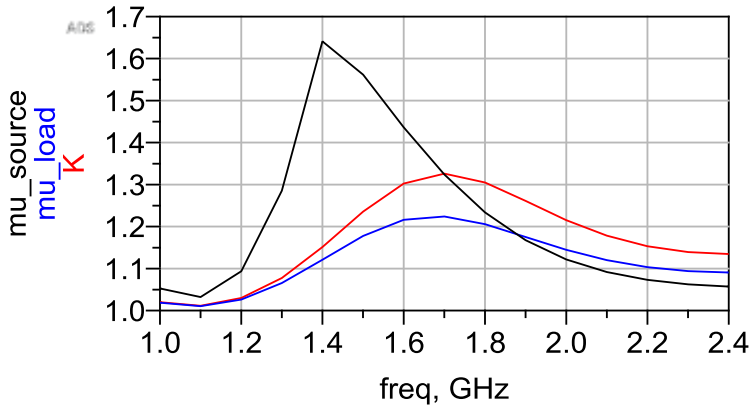


Figure 13: Stability Factor, K Geometric stability factor smu_source and mu_load

4. Conclusion

The majority of research papers use either SiGe (BiCMOS) or CMOS transistors to design LNAs, as can be seen. However, the GaAs-pHEMT is utilized in the design of the majority of commercial LNAs. Additionally, few commercial LNAs have a noise figure of less than 0.5 dB. The silicon process has a higher integration solution than other transistor processes. Due to their superior performance, the GaAs-HEMT and other BiCMOS (mostly SiGe) processes have dominated the RF industry up until recently. However, the CMOS process is now beginning to emerge. It is possible to observe the trade-off between the noise figure, linearity, gain, and power. With some compromises regarding power, gain, and a few other parameters, a design with a low noise figure and good linearity is possible. The purpose or application for which it is used determines the requirements of an LNA design. Most of the time, base stations look for low NF and good linearity, but WLAN, Bluetooth, GPS, and a few other applications look more for linearity and a noise figure that is quite acceptable.

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