MINIMISATION OF DEVICE COUNT IN NOVEL MULTILEVEL INVERTER COMPARED TO CONVENTIONAL MULTILEVEL INVERTER TOPOLOGY TO REDUCE THE COST

A.Lokeshwar Reddy[1], R. Hariharan[2*]

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Abstract

Aim: The aim of this proposed novel multilevel inverter (MLI) topology is to minimize the device count compared with conventional multilevel inverter topology thereby reducing the cost.
Materials and Methods: Novel MLI topology is compared with conventional MLI. Sample size is calculated using Gpower software and determined as 14. Gpower is taken as 0.8.
Results: For 21 level output voltage the conventional MLI topology requires 40 devices (switches and diodes) whereas novel MLI topology requires 23 devices (switches and diodes). Significance value is observed as 0.012 ($p<0.05$, statistically significant).
Conclusion: It is observed that the Novel multilevel inverter topology utilizes less device count compared to conventional MLI topology which results in reduced cost.

Keywords: Novel Multilevel inverter, Conventional Multilevel inverter, Pulse width modulation, switching sequence, Power Electronics

[1]Research Scholar, Department of Electronics and Communication Engineering, Saveetha School of Engineering Saveetha Institute of Medical and Technical Sciences, Chennai, Saveetha University, Chennai, Tamil Nadu, India -602105.
[2*]Project Guide, Department of Electronics and Communication Engineering, Saveetha Institute of Medical and Technical Sciences, Chennai, Saveetha University, Chennai, Tamil Nadu,India-602105.

1. Introduction

In recent years, multilevel has become increasingly important in generating the required output voltage in grid-connected photovoltaic systems. (Silva et al. 2019) this study looks at two multilevel inverter topologies in order to reduce system costs by proposing new inverter topologies with fewer devices than conventional MLI topologies (Babaei, Kangarlu, and Mazgar 2012; Kavali and Mittal 2016)). The proposed MLI topology provides higher output voltage with lower harmonics and loss, resulting in high system performance (Kaczmarek and Jama 2014). Multilevel inverters are used in grid-tied systems, dc drive applications, photovoltaic systems, and other applications (Abed 2018)(Rajalakshmi and Rangarajan 2019)(Abed 2018).

Various studies have been conducted to improve the performance of the MLI topology, with approximately 1078 papers published in IEEE and Google Scholar. This work proposes a three-stage Modified Multilevel Inverter (MMLI) geography with a diminished switch count for nine levels, and the geography is dissected utilizing different PWM techniques. The Total Harmonic Distortion (THD) level of this geography is researched using PWM strategies for symmetric and awry DC voltage sources. (Rajalakshmi and Rangarajan 2019). The work proposes new bilaterally symmetrical and uneven construction electrical converter topologies. as compared to standard multilevel inverters and alternative non-conventional topologies, the projected multilevel inverters use a smaller variety of change devices for a given number of output voltage levels (Babaei, Kangarlu, and Mazgar 2012)(Phyu, Aung, and Quan 2016), (Nourinezhad and Soleymani 2015)(Babaei, Kangarlu, and Mazgar 2012). This work compares numerous management themes in terms of Total Harmonic Distortion (THD) within the output voltage and utilization issue of power devices. The doctor's degree in the curving Pulse breadth Modulation-Phase Disposition (SPWM-PD) scheme with variable radio wave magnitude is found to be all-time low of all control schemes (Babaei, Kangarlu, and Mazgar 2012; Kavali and Mittal 2016). In this work, an original flowed transformer staggered inverter is proposed. In the proposed geography, its quantity is diminished to switch gadgets. Lessening the quantity of exchanging gadgets, which additionally implies diminishing the quantity of door drivers, brings about a more modest size and lower execution costs. Exchanging power misfortunes are additionally diminished in this geography. The proposed inverter utilizes the specific symphonious disposal (SHE) procedure to deliver a top notch yield voltage (Khounjahan, Banaei, and Farakhor 2015).

Our institution is passionate about high quality evidence based research and has excelled in various domains (Vickram et al. 2022; Bharathiraja et al. 2022; Kale et al. 2022; Sumathy et al. 2022; Thanigaivel et al. 2022; Ram et al. 2022; Jothi et al. 2022; Anupong et al. 2022; Yaashikaa et al. 2022; Palanisamy et al. 2022). Conventional MLI structure has high harmonics, loss and provides less efficiency . The aim of this research is to propose a novel MLI topology by minimizing the device count which results in a cost effective system and improving the performance.

2. Materials and Methods

This research was carried out in the Saveetha School of Engineering's Power Electronics Laboratory. Using previous study results, the sample size was calculated (Vemuganti, Sreenivasarao, and Kumar 2017). Two MLI topologies were compared, and their sample sizes were calculated using G power software; it was determined that each method has 7 samples, and a total of 14 sample tests were performed (g power setting parameters: statistical test-difference between two independent means, =0.05, power=0.80, effect size d=0.5). The Matlab simulink software is used to simulate the system.

Conventional MLI topology

The existing topology is a conventional multilevel inverter extensively used with symmetrical and asymmetrical configuration. The major drawback of existing topology is it requires more number of switches or devices which increases the size and cost of the system. The circuit describes the configuration and staircase building of voltage building of topology with reduced switches in the multilevel inverter. In this work, a clever flowed transformer staggered inverter is proposed. In the proposed geography, its quantity is decreased to switch gadgets. Lessening the quantity of exchanging gadgets, which likewise implies diminishing the quantity of door drivers, brings about more modest size and lower execution costs. Exchanging power misfortunes are additionally decreased in this geography. The proposed inverter utilizes the specific consonant disposal (SHE) strategy to deliver a top notch yield voltage (Vemuganti, Sreenivasarao, and Kumar 2017; Gupta and Bhatnagar 2017).

Proposed MLI topology

A separate degree generator and polarity generator are blanketed withinside the proposed topology. As a result, this topology necessitates using an H-

bridge inverter to invert the polarity of the extent generator module. The degree generator is made of an enter DC source, 3 equal-valued capability dividing capacitors, diodes, and unidirectional – blocking – bidirectional – undertaking strength switches (S1, S2, S3, and S4), while the polarity generator is made of 4 unidirectional – blocking – bidirectional – undertaking switches (S1, S2, S3, and S4) (T1, T2, T3 and T4). Because this topology necessitates using a capacitor to divide the capability of the DC bus, it necessitates using extra manage circuitry to hold the fee stability of the capacitors. A resonant switched capacitor converter (RSCC) is used to stability the voltages of the capacitors. The proposed topology's degree be counted number may be expanded absolutely with the aid of using cascading its fundamental module and accordingly utilising its modularity feature. When as compared to the traditional CHB topology for the equal voltage degree in output, the proposed topology notably reduces the variety of DC sources, switches, and motive force circuits ((Mohan Mathur and Varma 2002).

Statistical Analysis

The statistical analysis is done by using SPSS tools for obtaining the performance of the conventional multilevel inverter topology and the novel multilevel inverter. Statistical features such as mean, standard deviation and standard mean error are obtained for both the topologies using the statistical tools. Number of levels is an independent variable and device count and cost are dependent variables. Independent T test analysis is performed in this research work.

3. Results

Proposed topology has been simulated using MatLab software and the analysis is carried out. Table 1 represents the device count requirement for different levels of output voltage. Table 2 reveals the group statistics analysis of proposed MLI and conventional MLI with mean values of 11 and 28 respectively. Table 3 shows the independent sample T test analysis based on device count. Significance value is observed as 0.012 ($p<0.05$) which is statistically significant.

Figure 1 shows the conventional multilevel inverter topology. Figure 2 represents the proposed MLI topology with reduced device count. Figure 3 shows the bar chart analysis of both topologies. It is inferred that the proposed MLI topology requires low device count compared to conventional MLI structure. Reduced device count reduces the cost of proposed MLI topology.

4. Discussion

In this research work the MLI topology has been modified by reducing the number of device counts compared to conventional MLI structure. The cost of the proposed topology is also less due to low device count.

By combining 2 well-known topologies, cascaded H-bridge construction electrical converter and multi-string multilevel inverter, and proposing a replacement topology, Novel construction Inverter. a completely unique multilevel inverter is projected to scale back device count so as to reduce hardware size, cost, and quality (Raval and Ruvavara 2018). A Novel structure electrical converter is planned during this work. As compared to existing structure electrical converter topologies, the proposed Novel structure electrical converter topology needs fewer parts equivalent to switch devices and driver circuits to get a given range of output voltage levels. This reduces the dimensions and value of the inverter system even further (Maity, Roy, and Saha 2017). This work proposes a unique switched electrical device construction electrical converter structure (SCMLI). In comparison to alternative existing topologies, the planned topology provides a lot of output voltage levels whereas having a lower device count. The comparison is completed in numerous aspects, resembling the quantity of switches, dc power supplies, capacitors, and diodes accustomed to generate specific output voltage levels (Debatal et al. 2018). A novel multilevel inverter topology with a low device count is proposed in this work. With nine switches and four unbalanced DC sources, it can generate a 13-step output voltage. It is easily expandable to a greater number of voltage levels while using fewer power components and fewer semiconductor switches (Debatal et al. 2018; Kakar et al. 2019).

The limitations of the proposed topology, has high cost and needed high maintenance due to the complex design. The future scope of the proposed topology is to simplify the circuit design of the Novel Multilevel Inverter in order to reduce the cost and maintenance of the system.

5. Conclusion

Based on the analysis it is concluded that proposed MLI topology required less device count compared to conventional MLI topology. For 21 level output voltage the proposed MLI topology requires 23 devices whereas existing topology requires 40 switching device count. Due to less device count in proposed topology the cost is also reduced. The significance value is obtained as 0.012 ($p<0.05$) based on T test analysis which is statistically significant within the limit of study

Declarations

Conflict of Interest

No conflict of interest in this manuscript.

Authors Contribution

Author ALR was involved in data collection, data analysis, and manuscript writing, while author RH was involved in conceptualization, data validation, and manuscript critical review.

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Tables and Figures

Table 1. Device count of proposed and conventional MLI topology for various levels.

S.No	No.of levels	Device Count	
		Conventional MLI	Proposed MLI
1	9	16	11
2	11	20	13
3	13	24	15
4	15	28	17
5	17	32	19
6	19	36	21
7	21	40	23

Table 2. Group Statistical analysis of proposed and conventional MLI. Mean Stress, Standard deviation and standard error values are obtained for 14 sample data sets.

Group Statistics					
Group		N	Mean	Std. Deviation	Std. Error Mean
Device Count	P-MLI	7	11.0000	2.16025	0.81650
	CHBMLI	7	28.0000	8.64099	3.26599

Table 3. Independent sample T-test t is performed for the two groups for significance and standard error determination. Significance value is observed as 0.012 ($p<0.05$, statistically significant).

Independent Samples Test	
Levene's Test for Equality of Variances	T-test for Equality of Means

		F	Sig.	t	df	Sig. (2-tailed)	Mean Difference	Std. Error Difference	95% Confidence Interval of the	
Device Count	Equal variances assumed	8.796	0.012	-5.050	12	0.000	-17.00000	3.36650	-24.33498	-9.66502
	Equal variances not assumed			-5.050	6.747	0.002	-17.00000	3.36650	-25.02140	-8.97860

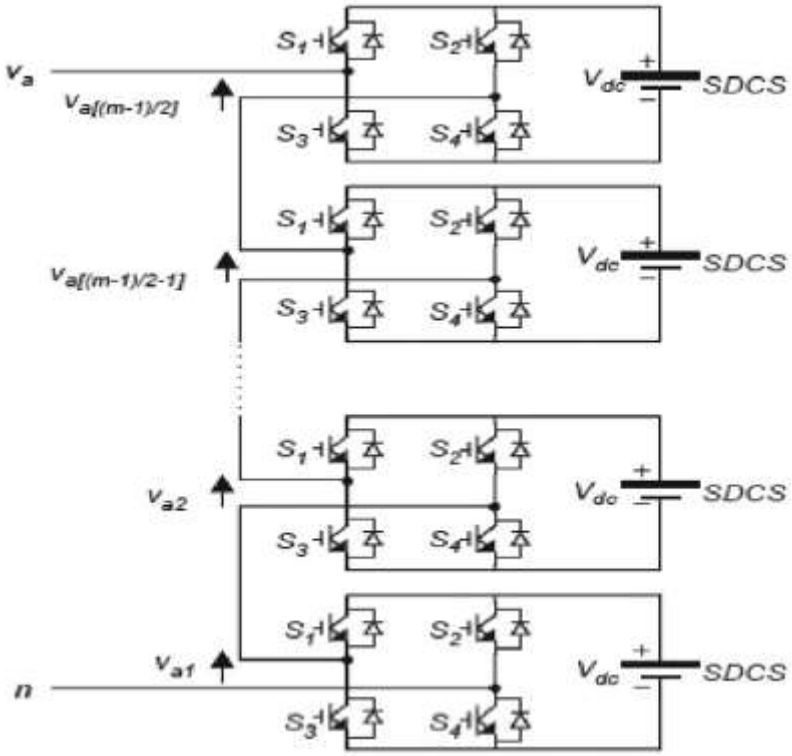

Fig. 1. Conventional MLI topology

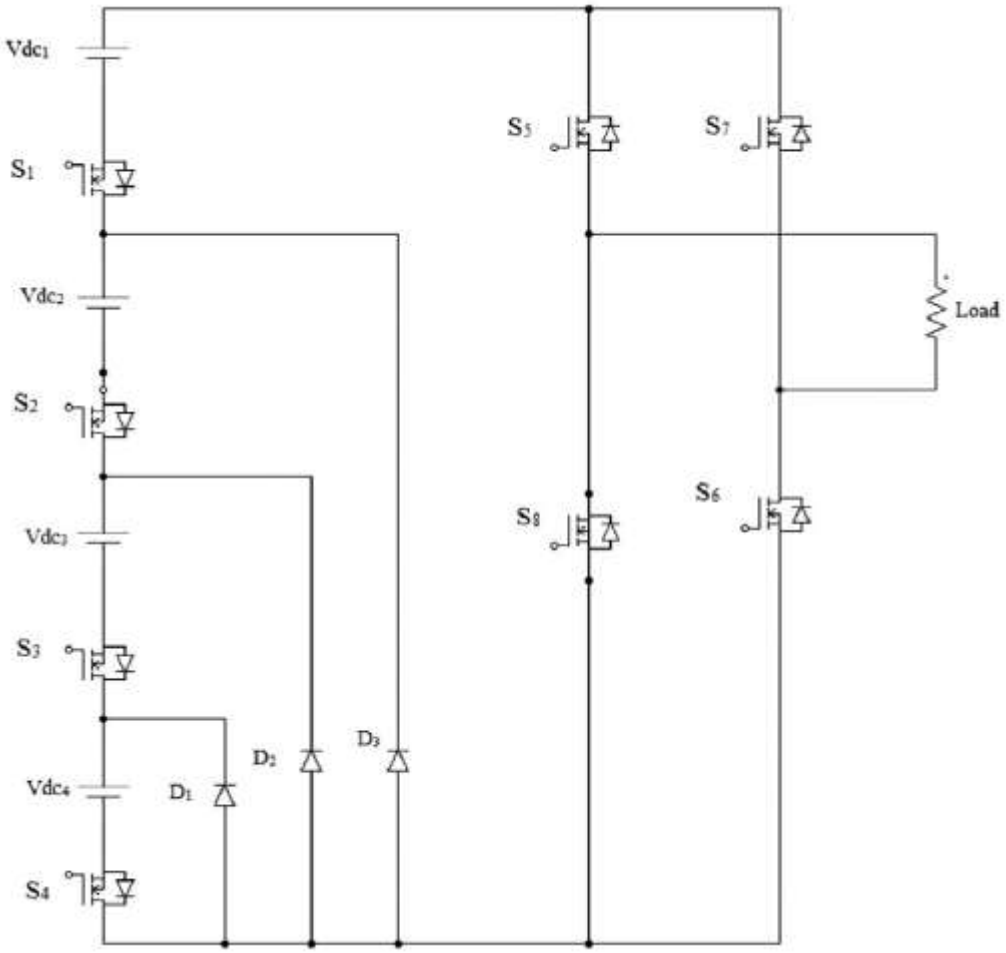

Fig. 2. Proposed MLI topology

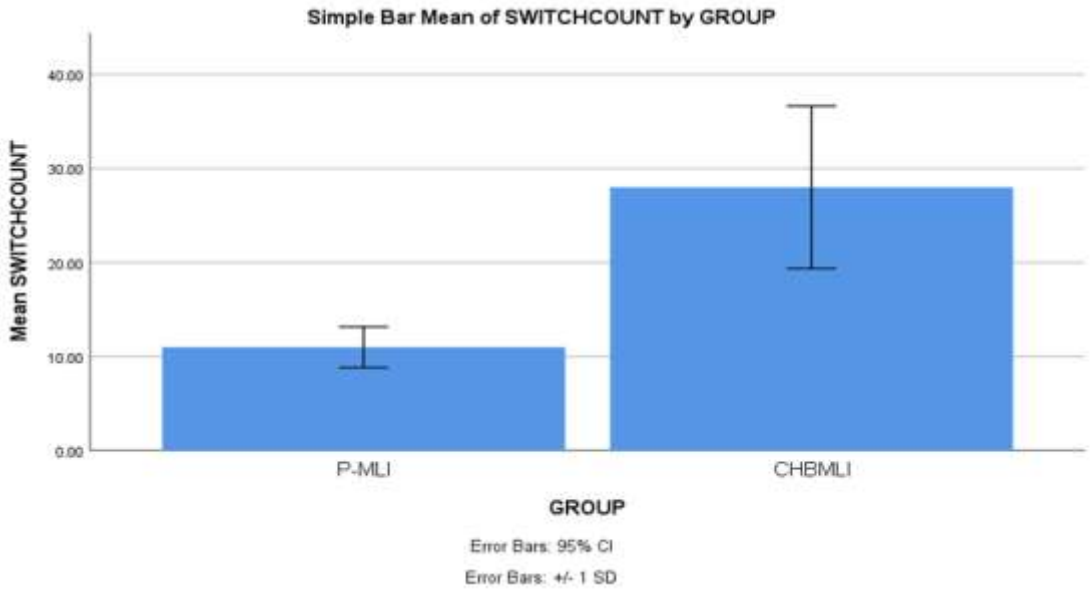

Fig. 3. Bar Chart Comparison of P-MLI and CHBMLI. Proposed MLI requires less device count compared to CHBMLI. Standard deviation range is less in P-MLI. X Axis: PMLI and CHBMLI topology, Y Axis: Device Count with ± 1SD.