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MULTILEVEL IMAGE DECOMPOSITION BASED ON THE HARR WAVELET TRANSFORM

T.R Dinesh Kumar[1], S. SivaSaravana Babu[2], R.Chandru[3], S.Durai Murugan[4], S.Yokesh Kumar[5], B.Udhay Kumar[6], S.Yeswanth[7]

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Abstract

In recent decades the demands for area efficient discrete wavelet transform (DWT) has been emerging steadily within the field of digital image & vision analysis. Among other transform model wavelets allows to decomposing the inputs into various bands in accordance with the frequency ranges. In general discrete Wavelet Transform (DWT) requires large number of multiplication units for multi level transformation. But HAAR wavelet requires only accumulation units since it comprise of wavelet coefficients with smaller integers (+1 or -1). In this paper optimized HAAR wavelet is introduced with Kogge–Stone based parallel-prefix topology for accumulation. This prefixbased model offers high-speed solution for HAAR DWT in image processing applications. Here in this work Modified Carry Correction block is introduced to optimize the KSA PPA and optimal clock Dividers/Reset Counter is used for data flow control. To maximize thesystem performance with improved reliability and the applicability of proposed design here configurable critical path delay optimization is introduced which can allows DWT to operate at variable rate. The flexible hardware architecture of multi-level decomposition is presented in this research. Discrete.For image compression applications, the Wavelet Transform (DWT) is suggested to remove extraneous data from the sent images or video frames over the wireless channel. The Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL)-based methodology is used to describe and synthesise the DWT architecture. With a few minor adjustments, the design can be implemented on any target Field Programmable Gate Array (FPGA) device. It supports images with resolutions of 64 x 64, 128 x 128, 256 x 256, and 512 x 512 pixels and has a seven-level deconstruction capability. n. The Fast Haar Wavelet Transform (FHWT) is used to reduce computational complexity. The 2D DWT multilevel FPGA core's decreased resource utilisation can be used to work around the severe hardware limitations of a variety of wireless and mobile device applications.

INDEX TERMS: Parallel Prefix accumulation (PPA), HAAR DWT, clock divider, FPGA,path delay optimization, Multilevel decomposition, 2D DWT, FHWT, VHDL, FPGA.

trdinesh@velhightech.com [1], sivasaravanababu@velhightech.com [2], rchandru489@gmail.com [3], murugandurai19@gmail.com [4], yokeshsellappa2004@gmail.com [5], udhay1303@gmail.com [6], yeswanths788@gmail.com [7]

[1,2]Assistant Professor, Department of Electronics and Communication Engineering

[3,4,]UG Student, Department of Electronics and Communication Engineering

Vel Tech High Tech Dr. RangarajanDr. Sakunthala Engineering College, Chennai, India.

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I. INTRODUCTION

The advent of wide range of image modalities inbiomedical application devices the demands for high performance accumulators and distributive arithmetic models and associated digitalcomponent designare emerging steeply for digital filter design (FIR) filtering [1], discrete wavelet transform (DWT) [2] and FFT computation [3] etc. On the other side carry free prefix topology based arithmetic models arepredominantly used in many next generation wireless devices and high performance digital system for its improved path delay reduction and parallel processing metrics [4-5].

The requirement to process and send a massive amount of visual data wirelessly will be one of the biggest problems for next-generation wireless access technologies. Memory and bandwidth use are the key constraints in image transmission and storage applications [1].Compression techniques can be used to lower the quantity of data being transmitted over the wireless channel as a way to alleviate this complication. These methods concentrate on increasing compression ratios while minimising image quality loss. The Joint Photographic Experts Group is the most well-known and widely used picture coding and decoding standard in the world today (JPEG). Unfortunately, JPEG uses the discrete cosine transform (DCT) kernel, which has significant disadvantages, particularly for low-bitrate applications [1] and [2]. There is a need to remove all of these restrictions and provide new, improved functionality as a result. It is suggested that JPEG 2000 be used to provide a new picture compression method based on the use of wavelet technology.The convolution approach, which is the original way of constructing finite impulse response (FIR) filter bank structures, has traditionally been used to perform the discrete wavelet transform (DWT) [3]. The lifting scheme (LS), based on the spatial construction of the wavelet, is a novel method. It is an extremely robust method, and [4] suggests factorising it.

Practically, the input signal is separated into odd and even indexed components as the LS's starting point. Finally, by altering this set of samples to be utilised in the following phase, the process of employing alternate prediction and updating processes is carried out. The JPEG2000 standard filters for lossy and lossless compression use the 9/7 and the 5/3 DWT lifting schemes, respectively. In contrast to the 9/7 filter's two predictions and two updating processes, the 5/3 filter only has one prediction and one updating process [5]. The choice of wavelet type has a significant impact on wavelet-based picture compression performance [6]. The Fast Haar Wavelet Transform (FHWT) is the wavelet considered in this paper for simplicity. The reasons are that it has superior qualities, such as quick processing and memory efficiency, which negate the need for additional capacity.

It is completely reversible and free of the edge effects that other wavelet transforms encounter. The Haar wavelet's methodological flaw is that it is not continuous and, consequently, not differentiable. Nonetheless, this characteristic may be useful for the analysis of signals with abrupt transitions [1] [5] [6]. Mobile and 2013 IEEE International Conference on Control Systems, Computing, and Engineering, November 29–December 1, 2013, Penang, Malaysia 978-1-4799-1508-8/13/$31.00 Wireless communication networks cannot use the current software compression algorithms, such as JPEG 2000. These algorithms demand very sophisticated hardware. The implementation of JPEG 2000 requires two steps: the first is the wavelet transform, and the second is the coding of the transformed components. This implementation is widely used in the literature [6]. As a result, the primary goal of this work is to describe the hardware for the Discrete Wavelet Transform (DWT), a crucial component of JPEG 2000 implementation.

Lately, FPGA technology has shown

promise as a low-cost design platform for high-performance systems. In order to reduce computing complexity, the FHWT algorithm candidate is built in VHDL using FPGA technology. The DWT equations are solved using the linear algebra method, which almost produces the same result while using significantly less resources [5] [7].

Moreover in many cases same PPA models are used to configure other arithmetic models. To optimize the path delay and associated computational complexity wide range of different prefix topologies with various path delay characteristics are introduced in many existing works. In general, the significant performance degradations are presented with bit width and carry approximation level. In particular for image processing applications the optimal MAC should comprise of optimized arithmetic modelfor high performance[6]. Moreover many existing works numerous types of several hardware optimization methods [7-8]are used to reduce the design complexity overhead and path delay propagation overhead with reduced critical path. In particularmultiplication in image processing applications [9-10] need both path delays as well complexity analysis in a large set.This DWT paper work is formulated as follows. Section II includes the detailed analyzes of prefix and DWTtransformation models and various image decomposition models used for biomedical applicationsand its FPGA hardware implementation. Section III discussed proposed HAAR DWT transform and associated prefix topologies which includes configurable clock divider and controller techniques Section IV summarize the comparative analyzes of proposed HAAR DWT with existing models through FPGA hardware synthesis. Section IV concludes the details.

II.RELATED WORKS

In this section includes the advantages of existing wavelet design models core and its implications on performance efficiency and reliability measures in image processing applications. In general both multipliers based and multiplier less arithmetic design comes with its own merits and associated performance tradeoff measures. In most cases performance trade-off is significant when multipliers are used for DWT transform. Implementation of multiplier less DWT core is introduced for improved path delay optimization with associated parametric performance constraints.

In [11] hybrid prefix adder is developed with speculative prefix carry generation tree where two post and prefix computation kernels are combined to formulate the path delay optimized carry signals and finally speculative carry approximation scheme is introduced to Ling adders which produces accumulation end results faster than all other prefix adders with less hardware complexity.

In [12] variable latency adder is developed based on Kogge-Stone topology and ends with highly stage-wise carry approximated path delay models and associated error correction blocks which is asserted in case of speculation fails and processed as post computation model. In order to overcome these limitations, a global carry signal is introduced in [6], which are asserted in during hierarchical carry propagationover successive tree structure. This global assertion can be used to suppress the accusation of error outcome during carry approximate using additional mux based bypass logic levels that maximize the overall system performance.

The variable latency adder (VLA) introduced in [13] reduces average addition time by using carry approximated speculation. Here during speculative prefix-processing stage the intermediate rows obtained from optimal path delay optimized parallel-prefix graph is formulated. This Pruned mid row eliminates and breaks the propagate carry chain for the most significant bit which gives considerable hardware complexity reduction. Speculative parallel-Prefix topology based MAC

designed in [14] is offered improved path delay metrics as compared to other well known high performance adders such as CSA and CLA.

In [15] proposed modified Carry Select Adder (CSLA) based on systolicprefix structure based Binary to Excess–1 converter (BEC). Comparative analyzes is carried out with generic BEC, and conventional prefix tree based topology model to validate the performance metrics of CSLA. The experimentation proves that the inclusion of BEC in KS based CSLA offers notable improvement in speed as compared to other competitive prefix models.

In [16] Han–Carlson adder (HCA) based high-performance Vedic multiplier is introduced for high-performance multiplier. Here vedic multiplier includes Urdhva–Tiryakbhyam sutra for partial product generation and usedspeculative parallel-prefix topology to design 64 bit multiplier. The results proves that the combination of PPA with vedic outperform all other existing vedic multipliers with different adders. For complex multiplication architectures, the efficiency is increased by three to times as compared to complex multiplication based existing booth recoding multiplier with associated partial product accumulation model.

Images	Original image	GAAHE	IDE	WTHE	Proposed algorithm
Figure 1	0.3039	0.5945	0.2968	0.4188	0.6602
Figure 2	0.3032	0.6067	0.2967	0.4163	0.6645
Figure 3	0.3065	0.6098	0.3001	0.4224	0.6657

It is currently indisputable that the 2D DWT is a suitable tool for image and video compression. In the literature, a number of computation scheduling architectures that use both combined lossy and lossless transforms to execute the multilevel 2D DWT have been presented [8], [9], [10], and [11]. A quick comparison of the lifting-based and convolution-based DWT executions with embedded hierarchical picture compression structures is given in [6].The row-column (RC) [3], line-based (LB) [22], and block-based (BB) [17] calculation schedules are the ones that are utilised most frequently in practical designs. In order to simplify the design and accelerate computation, a modified RC hardware 2D-DWT architecture is created in this study. [18] contains one of the early iterations of FHWT. The use of FHWT for signal analysis, image compression, and atmospheric turbulence analysis has been explored in [19]. The suggested architecture incorporates upgradeable, reconfigurable transform modules with multi-level resolutions, such as the 1D-DWT and 2D-DWT. The Cyclone II Altera DE2 FPGA Development Board simulates the VHDL model for the architecture description.

III .HIGHPERFORMANCE DWT TRANSFORM DESIGN

In DWT transformation input images are pre-processed with macro block conversion and applied wavelet transforms using orthogonal basis as follows.

$$W_s s(b) = \int_{+\infty}^{-\infty} f(t)\psi(\frac{t-b}{s})dt \qquad (1)$$

Here in order to maximize the transformation levels wavelet sequences are preprocessing using appropriate approximation techniques. Here only minimal number of DWT sequence are selected which comprise of both low and high pass filter coefficients finally band decomposed output is formulated using succeeded concatenation of DWT multi level decomposed output as shown in figure 1.

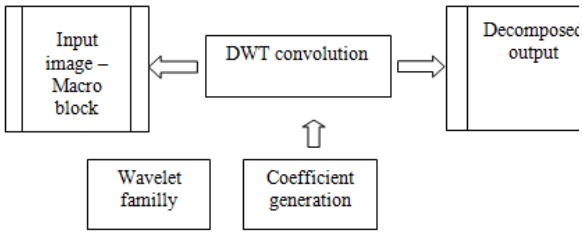


FIGURE1.General architecture of DWT in image processing

Here DWT transform of level M is formulated by N+1 g and h coefficients and, in most cases, require N+1 multipliers and associated accumulators to perform DWT transformation. In transform domain DWT architecture the wavelet coefficients are formulated based on given wavelet family which includes both approximated and detailed coefficients of the wavelet function are called decomposition model. The main drawback of DWT is the increased amount of computation needed to process a input image through the DWT.

TABLE 1. Contrast of CT images

According to Table 1, the GAAHE algorithm imtroves contrast by about 100%, outperforming IDE and WTHE in this regard. Nonetheless, the suggested method outperforms GAAHE by an average of 9.96% while doing better in terms of visualisation. As a result, the suggested method performs better than current algorithms.

As shown in Table **1**, GAAHE algorithm improves contrast by 100 percent nearly, which performs well than IDE and WTHE in contrast enhancement. But the proposed algorithm improves the image contrast by an average of 9.906% than GAAHE algorithm, while performs superior in visual. Hence, the performance of the proposed algorithm is better than existing algorithms.

A. DA BASED APPROACHES

In DA models multiplication operation is performed using shift come accumulation or approximated designs models where significance ofmultiplier is suppressed which exhibits a improved energy and area efficiencyas compared to conventionalcore multiplier models [6]. In section III, the parallel strategy for DA-based multiplication is explained. This section introduces the pipelining technique on top of the parallel DA approach in order to speed up multiplication even more. LUTs in table1 are further separated into four sections in order to use the pipelining technique. After receiving the output from the LUT, the shift/addition unit is processed to produce the multiplication results

In general, approximated HAAR DWT and prefix accumulation based DWT transform has following numerical metrics.

1) Multi level decomposition can performed using coefficient matrix which includes only +1 and -1 which can offer considerable complexity reduction.

2) the accumulation DWT transformation results can be performed using carry free prefix accumulation to solve trade off path delay constrains which is obvious in any DA models.

3) Path optimized carry propagationwith associated data flow controllercan improve speed of PPA operation with appropriate data accessibility.

The survey section includes all relevant works which are focused on path delay optimization and DA based DSP models. The issues and challenges related to any DA models irrespective to the applications are explored have and various solutions provided to mitigate these issues also discussed in details. The novel methodologies which can overcome these limitations are described in the next chapter.

B. PARRALEL PREFIX ACCUMULATION

Here kogge stone prefix methodology used in this model includes approximation based complexity reduction which is accuracy-related thresholds that are essential to meet in image processing applications. Here due

to some parametric word length constrains the end results are not always accurate in nature. The major cause of quality loss is due to the accumulation of computational errors which gives opportunity of incorporating the approximation design approaches. Approximation can be used only in designs with inexact circuits which has limited sensitivity towards end results. Most cases digital systems are error tolerance in nature where approximate designs are emerged as prominent design measures to optimize energy consumption and hardware complexity overhead. Approximation is performed in both addition and multiplication components which the most basic functional units in this image processing applications.

$$g_i = a_i \bullet b_i$$

$$p_i = a_i \oplus b_i$$

$$G^l_{i:k}, P^l_{i:k} = (G^{l-1}_{i:j} + P^{l-1}_{i:j} G^{l-1}_{j:k}, P^{l-1}_{i:j} P^{l-1}_{j:k} \ldots\ldots\ldots k \le j \le i; l = 1,2,\ldots\ldots, m$$

$$C_{i+1} = G^m_{i:0} + P^m_{i:0} C_{in} \ldots\ldots\ldots i = 0,1,2,\ldots\ldots, n-1$$

$$S_i = p_i \oplus C_i \ldots\ldots\ldots i = 0,1,2,\ldots\ldots, n-1$$

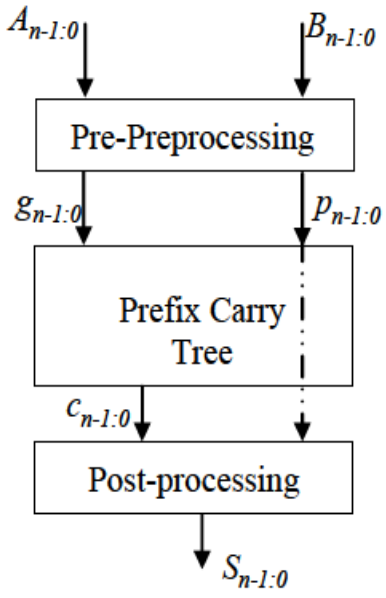


FIGURE 2. Parallel Prefix Adders

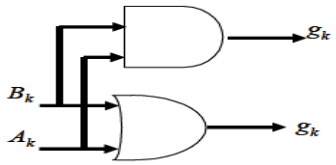


FIGURE 3. Gate level Logic used for Pre- processing andpost processing

C. HIGH PERFORMANCE MODELS

Here during accumulation carry approximation isused dynamically for given input and that can be easily used for path delay optimization without using pipeline management schemes. Moreover more than one carries are generated using multiple path sets to allow optimal computation during DWT transformation. In such systems, transformation level is very high as compared single carry compound PPA cores where same carries are used for throughput the transformation stored which also stored in memory.

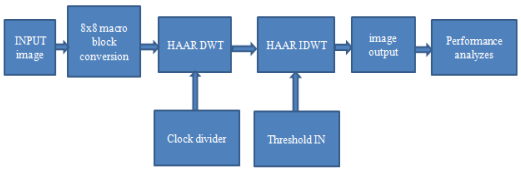
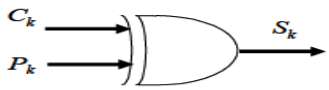


FIGURE 4.Proposed HAAR DWT for image processing application

Area efficient design

The basic computations involved in proposed HAAR DWT include only simplified elements which includes +1 and -1 which is not complicated image processing steps which requires least computational complexity overhead. And also image statistics used for DWT modeling is also not uniform across different image modalities. The computational complexity trade-off is always occurs with respect to attainable transformation margin in any integer based DWT system and its trade-off level is varying according to the coefficients adopted for application.



IV.EXPERIMENTAL RESULTS

Here to prove the performance metrics of proposed prefix topology enabled HAAR DWT is compared over conventional multiplier based DWT model and proved its superiority measures both in terms path delay and complexity reduction measures.

Image DWT model	Area(LE's used)	Fmax (MHz)
Existing optimal DWT	457	322.16 MHz
Proposed path delay optimized DWT	565	332.89 MHz

As compared to existing KSA based accumulation and associated clock divider based data flow control the proposed path delay optimized PPA showed significant path delay reduction with least possible hardware complexity overhead. The proposed HAAR DWT core is designed using the Verilog HDL and hardware tranalsted using INTEL QUARTUS II FPGA synthesizer for comparative analyzes.

Simulation Results

In order to verify the functionality of the proposed HAAR DWT core input testbench stimulus is generated using exhaustive test bench which includes MATLAB generated digital image. Here 8x8images is decomposed and memoryis configured to process the digital image. Here both DWT and IDWT are connected with hierarchical register to regulate the data flow and queue the data input.

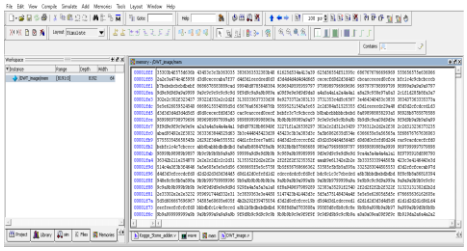


FIGURE 6. DWT decomposed output image

FIGURE 5. HAAR DWT core input testbench stimulus

Table 2 Performance comparisons between path delaysoptimized HAAR DWT vs.existing HAAR DWT using

FGPA

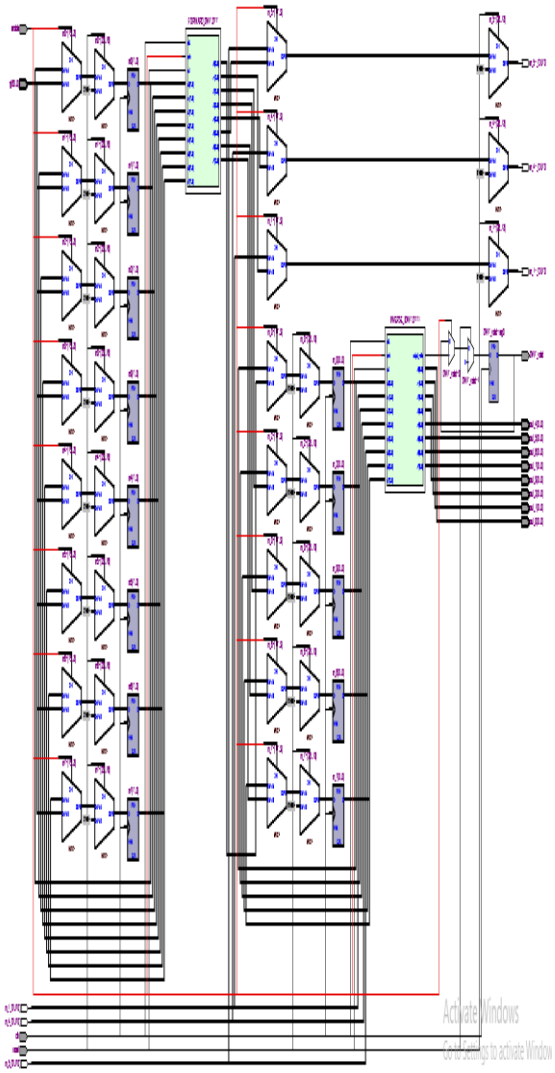


FIGURE 7. Optimized DWT Architecture

V. CONCLUSION

Here in this paper path delay optimized KSA based HAAR DWT implementation for modified wavelet transformation architecture with improved performance measures. Here configurable clock dividerbased controller is used and evaluated to regulate the data flow. Here, in proposed path delay efficient DWT architecture configurable clock divider is used as potential replacement to existing data flow controller and buffer, which comprise of configurable delay lines which can assert, control signals. By merging this optimal clock dividing operation and associated data buffering path delay is significantly reduced. From the experimental analyzes it is validated that the proposed path delay optimized HAAR DWT based design offered improved performance efficiency as compared to convention HAAR DWT model.

The 2DDWT is intended to be employed in this hardware architecture's low-power image compression system. The FHWT of DWT (FDWT and IDWT) algorithm utilising the VHDL approach is the main focus of this study. The gate-level architecture of the design, which is ready to be executed in the hardware environment, was also generated using this VHDL code. The hardware module applies 2D DWT to four different-sized pictures. The results of the synthesis process revealed that the four variants have the same maximum frequency of 50 MHZ and 700 slices of Altera DE2 logic. The higher decomposition level reveals greater errors in addition, subtraction, and division by two calculations.

Using the whole variational framework and taking into account the specified complex noise model, the CT image is divided into two layers: a low-frequency structural layer with weak contrast and a high-frequency detail layer with complex noise. The image is transformed to the wavelet domain using the wavelet transform, with the high-frequency detail layer as the target. The enhanced detail layer is created by processing and reconstructing the wavelet coefficient of noise. Due to the low contrast of the low-frequency structure layer, the adaptive polarisation histogram adjustment and Gaussian filter are used to create the contrast-enhanced structure layer by analysing the histogram characteristic. To create the enhanced image, the structural layer and enhanced detail layer are combined and sharpened.

This paper proposes an image enhancement algorithm that combines a variation framework with the wavelet transform in order to improve the characteristics of lung CT images, such as poor contrast, complex noise, and artificial artefacts. This algorithm

performs better than existing algorithms in terms of both objective indicators and subjective visual effects. Using lung CT scans, experiments confirm the suggested algorithm's efficacy and robustness.

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